1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
8	0003549590	ENGINEERING RELEASED	2014-12-19

X304 MLB SCHEMATIC - DVT

Fri Dec 19 12:14:48 2014

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45	58	Thermal Sensors	YHARTANTO_J44	01/07/2013
46	60	Fan	J41	10/23/2012
47	61	SPI Debug Connector	YHARTANTO_J44	01/09/2013
48	62	Audio: Codec,Analog	JCURCIO_J44	05/13/2013
49	63	Audio: Codec,Digital	JCURCIO_J44	07/25/2013
50	64	Audio: Speaker Amps	DIRK_J44	01/09/2013
51	65	Audio: Jack Support	JCURCIO_J44	07/25/2013
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53	70	DC-In & Battery Connectors	YHARTANTO_J44	01/09/2013
54	71	PBus Supply & Battery Charger	AHARTMAN_J52	11/06/2013
55	72	CPU VR12.6 VCC Regulator IC	J41	10/23/2012
56	73	CPU VR12.6 VCC Power Stage	J41	10/23/2012
57	74	LPDDR3 Supply	J41_MLB	05/21/2013
58	75	5V & 3.3V Power Supply	J14	10/23/2012
59	76	1.05V Power Supply	AHARTMAN_J52	10/29/2013
60	77	LCD & KBD Backlight Driver	SHART_J44	11/20/2012
61	78	Misc Power Supplies	AHARTMAN_J52	11/06/2013
62	79	X239 Power Supply	AHARTMAN_J52	11/06/2013
63	80	Power FETs	J41	10/23/2012
64	81	Power Control	AHARTMAN_J52	11/06/2013
65	83	eDP Display Connector	GKOO_J52	05/04/2014
66	95	RIO Connector	GKOO_J52	05/01/2014
67	97	Display Mux: HDMI vs DP	SRAMAN_J44	01/29/2013
68	100	Power Aliases	SHART_J44	01/14/2013
69	102	Signal Aliases	SHART_J44	11/19/2012
70	103	Memory Bit & Byte Swizzle	AHARTMAN_J52	10/29/2013
71	104	Functional & ICT Test	GKOO_J52	12/06/2013
72	110	PCB Rule Definitions	YHARTANTO_J44	12/14/2012
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74	112	USB Constraints	YHARTANTO_J44	01/07/2013
75	113	PCH Constraints	YHARTANTO_J44	01/08/2013
76	114	Memory Constraints	YHARTANTO_J44	01/02/2013
77	115	TBT,DP,HDMI Constraints	GKOO_J52	12/06/2013
78	116	Camera Constraints	YHARTANTO_J44	01/09/2013
79	117	SMC Constraints	YHARTANTO_J44	01/02/2013
80	118	Project Specific Constraints	YHARTANTO_J44	01/04/2013
81	119	PCIe Constraints	YHARTANTO_J44	01/13/2013
82	120	Reference	J14	10/23/2012

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-1573	1	SCHEM,MLB,X304	SCH	CRITICAL	
820-4924	1	PCBF,MLB,X304	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,X304

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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BOM Groups

BOM GROUP	BOM OPTIONS
X304_COMMON	ALTERNATE,COMMON,X304_COMMON1,X304_COMMON2,X304_COMMON3,X304_COMMON4,X304_PROGPARTS
X304_COMMON1	TBTHV:P15V,SKIP_5V3V3:AUDIBLE,PANEL:NEW,SSD_CLKREQ:BI
X304_COMMON2	EDP,EDP_LS_CAP,CAMERA_3V3:S0,CAM_WAKE:NO,CAM_XTAL:NO,VCORE_FETS
X304_COMMON3	XDP,SAMCONN,BKLT:PROD,CPUTHRM:ALRT,LOADRC:NO,OTHERRC:NO,DDRRC:NO,TBTRC:NO,BMONRC:NO,TPADRC:NO
X304_PROGPARTS	SMC_PROG:PROTO0,BOOTROM_PROG,TBTROM_PROG
X304_DEVEL:ENG	ALTERNATE,ENGISNS,XDP_CONN,DBGLED
X304_DEVEL:DVT	ALTERNATE,ENGISNS,XDP_CONN,S0PGOOD_ISL
X304_DEVEL:PVT	ALTERNATE
ENGISNS	LOADISNS,OTHERISNS,DDRISNS,TBTISNS,BMONISNS,TPADISNS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00107	1	CPU,BW,SR26K,PRQ,F0-B2,2.7,28W,1.05,1168	U0500	CRITICAL	CPU_BDW23:2.7G
337S00108	1	CPU,BW,SR26H,PRQ,F0-B2,2.9,28W,1.1,1168	U0500	CRITICAL	CPU_BDW23:2.9G
337S00109	1	CPU,BW,SR26E,PRQ,F0-B2,3.1,28W,1.1,1168	U0500	CRITICAL	CPU_BDW23:3.1G

DVT

998-7866	1	INTERPOSER,BGA116BP, SINGLE SIDE	U0500	CRITICAL	CPU_SOCKET
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1264	1	IC,BCM15700A2KFEB4G,S2 CMRA,8X8,208FCBGA	U3900	CRITICAL	
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
376S00036	2	MOSFET,N-CH,30V,52A,5.9MO,3.3X3.3 DFN8	Q7310,Q7320	CRITICAL	VCORE_FET:ONSMI
376S00037	2	MOSFET,N-CH,30V,64A,3.5MO,3.3X3.3 DFN8	Q7311,Q7321	CRITICAL	VCORE_FET:ONSMI

Programmables (All Builds)

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00192	1	T29,EPROM,FALCON RIDGE (V27.1) EVT2,X304	U2890	CRITICAL	TBTROM_PROG

SMC

341S3982	1	IC,SMC-B1,EXT(V2.21A5) PROTO 0,X304	U5000	CRITICAL	SMC_PROG:PROTO0

EFI ROM

341S00235	1	EFI ROM,MLB (V0145) DVT,X304	U6100	CRITICAL	BOOTROM_PROG

Variable BOM Groups

BOM GROUP	BOM OPTIONS
X304_COMMON4	SMCBOARDID:16

Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-1314	1	X304 MLB COMMON BOM	BASE	CRITICAL	BASE_BOM
985-1319	1	X304 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-1318	1	VCORE FET,VSHY,X304	VCOREFETS	CRITICAL	VCORE_FETS

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_16G_HYNIX_1600	16G_HYNIX_1600,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_16G_HYNIX_1866	16G_HYNIX_1866,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_8G_HYNIX_1600	8G_HYNIX_1600,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_8G_HYNIX_1866	8G_HYNIX_1866,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_4G_HYNIX_1600	4G_HYNIX_1600,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_4G_HYNIX_1866	4G_HYNIX_1866,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_16G_ELPIDA_1600	16G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_16G_ELPIDA_1866	16G_ELPIDA_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_8G_ELPIDA_1600	8G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_8G_ELPIDA_1866	8G_ELPIDA_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_4G_ELPIDA_1600	4G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_4G_ELPIDA_1866	4G_ELPIDA_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_8G_SAMSUNG_1600	8G_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_8G_SAMSUNG_1866	8G_SAMSUNG_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_4G_SAMSUNG_1600	4G_SAMSUNG_1600,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_SAMSUNG_1866	4G_SAMSUNG_1866,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00068	08	CPU
337S00069	08	CPU
337S00070	08	CPU
337S00071	08	CPU
353S00200	07	TPAD ELEC FUSE
333S0786	07	SYS MEMORY HYNIX
333S0784	07	SYS MEMORY HYNIX
333S0792	07	SYS MEMORY MICRON
333S0790	07	SYS MEMORY MICRON
333S00004	07	SYS MEMORY SAMSUNG
311S0597	02	KEYBOARD I2C EXPANDER
359S0197	01	GREEN CLOCK
338S1247	01	FALCON RIDGE
353S3931	01	TBT PWR MUX
353S3812	01	TBT MUX
353S3814	01	TBT MUX
353S00095	01	DDC CROSSBAR
353S3328	01	DDC CROSSBAR
343S0511	01	PCIE DELAY IC
338S1264	01	S2
333S0700	01	S2 MEMORY
333S0704	01	S2 MEMORY
353S3054	01	USB POWER/SAFETY
343S0649	01	SMC RESET CHIP
353S4080	01	AUDIO
353S2888	01	AUDIO AMPS
353S2958	01	AUDIO AMPS
353S2929	01	BAT CHARGER
353S00036	01	VR12.6 CONTROLLER
353S4160	01	BEN
343S0666	01	SAK, HDMI SELECT
341S3982	01	SMC
341S00192	01	T29 ROM
341S00235	01	EFI ROM

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0783	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	16G_HYNIX_1600
333S0784	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	16G_HYNIX_1866
333S0785	4	IC,SDRAM,29nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_HYNIX_1600
333S0786	4	IC,SDRAM,29nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_HYNIX_1866
333S0787	4	IC,SDRAM,29nm 8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_HYNIX_1600
333S0788	4	IC,SDRAM,29nm 8Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_HYNIX_1866
333S0789	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	16G_ELPIDA_1600
333S0790	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	16G_ELPIDA_1866
333S0791	4	IC,SDRAM,25nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_ELPIDA_1600
333S0792	4	IC,SDRAM,25nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_ELPIDA_1866
333S0793	4	IC,SDRAM,25nm 8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_ELPIDA_1600
333S0794	4	IC,SDRAM,25nm 8Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_ELPIDA_1866
333S00003	4	IC,SDRAM,23nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_SAMSUNG_1600
333S00004	4	IC,SDRAM,23nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_SAMSUNG_1866
333S00001	4	IC,SDRAM,23nm 8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_SAMSUNG_1600
333S00002	4	IC,SDRAM,23nm 8Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_SAMSUNG_1866

S2 DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0700	1	IC,SDRAM,4GBIT.DDR3L-1600,HUMA,96B BGA	U4000		

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SYNC_MASTER=SHART_J44 SYNC_DATE=11/27/2013

PAGE TITLE
BOM Configuration

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-1314	COMMON,MLB,X304	X304_COMMON
985-1319	DEV,MLB,X304	X304_DEVEL:ENG
639-00772	MLB,BDW2+3,2.7GHz,8GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_8G_HYNIX_1866
639-00773	MLB,BDW2+3,2.7GHz,16GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_16G_HYNIX_1866
639-00774	MLB,BDW2+3,2.7GHz,8GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_8G_ELPIDA_1866
639-00775	MLB,BDW2+3,2.7GHz,16GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_16G_ELPIDA_1866
639-00776	MLB,BDW2+3,2.7GHz,8GB-SM-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_8G_SAMSUNG_1866
639-00777	MLB,BDW2+3,2.9GHz,8GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_8G_HYNIX_1866
639-00778	MLB,BDW2+3,2.9GHz,16GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_16G_HYNIX_1866
639-00779	MLB,BDW2+3,2.9GHz,8GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_8G_ELPIDA_1866
639-00780	MLB,BDW2+3,2.9GHz,16GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_16G_ELPIDA_1866
639-00781	MLB,BDW2+3,2.9GHz,8GB-SM-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_8G_SAMSUNG_1866
639-00782	MLB,BDW2+3,3.1GHz,8GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_8G_HYNIX_1866
639-00783	MLB,BDW2+3,3.1GHz,16GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_16G_HYNIX_1866
639-00784	MLB,BDW2+3,3.1GHz,8GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_8G_ELPIDA_1866
639-00785	MLB,BDW2+3,3.1GHz,16GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_16G_ELPIDA_1866
639-00786	MLB,BDW2+3,3.1GHz,8GB-SM-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_8G_SAMSUNG_1866

BOM NUMBER	BOM NAME	BOM OPTIONS
639-00035	PCBA,MLB,NO CPU,X304	BASE_BOM,DEVEL_BOM,RAM_8G_HYNIX_1866
639-00036	PCBA,MLB,CPU SOCKET,X304	BASE_BOM,DEVEL_BOM,CPU_SOCKET,RAM_8G_HYNIX_1866
685-1318	VCORE FET,VSHY,X304	VCORE_FET:VSHY
685-00022	VCORE FET,ONSMI,X304	VCORE_FET:ONSMI

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
685-00022	685-1318		ALL		Onsemi alt to Vishay for CPU Core Mosfets
333S0704	333S0700		ALL		Elpida alt to Hynix for S2 Camera DDR3 Memory

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
376S1053	376S0604		ALL		Diodes alt to Fairchild
128S0311	128S0329		ALL		NEC alt to Sanyo
138S0739	138S0706		ALL		Samsung alt to Murata
197S0481	197S0480		ALL		Epson alt to NDK
152S0461	152S1645		ALL		Cyntec alt to Vishay
376S1080	376S0820		ALL		Diodes alt to On Semi
138S0725	138S0724		ALL		Samsung alt to Murata
376S00074	376S0855		ALL		Toshiba alt for Diodes Dual
376S1129	376S0855		ALL		NXP Alt for Diodes Dual
376S1089	376S1128		ALL		NXP Alt for Diodes Single
353S3452	353S1286		ALL		Maxim alt to Microchip
128S0364	128S0264		ALL		Sanyo 2nd Factory alt
107S0254	107S0241		ALL		Cyntec alt to TFT
138S0843	138S0674		ALL		Samsung alt to Murata (BKLT)
138S0846	138S0811		ALL		Samsung alt to Murata (BKLT)
197S0542	197S0544		ALL		NDK alt to TXC
197S0545	197S0544		ALL		Epson alt to TXC
107S0248	107S0250		ALL		TFT alt to Cyntec
127S0164	127S0162		ALL		Rohm alt to Vishay
353S4070	353S4069		ALL		Pericom alt to TI DP Mux U9750
353S4068	353S4069		ALL		NXP alt to TI DP Mux U9750
353S3814	353S3812		ALL		TI alt to NXP
311S0649	311S0541		ALL		ONsemi alt to Toshiba
138S0614	138S0578		ALL		Murata, TDK, Samsung, Taiyo Yuden alt to Murata, TDK
155S0694	155S0387		ALL		Murata alt to TDK
155S0660	155S0513		ALL		Murata alt to TDK
740S00003	740S0135		ALL		AEM alt to Tyco
138S0738	138S1101		ALL		Samsung alt to Murata for LCD BKL caps
353S00095	353S3328		ALL		Pericom alt to TI
311S00007	311S0426		ALL		Diodes alt to NXP
128S0398	128S0220		ALL		Kemet alt to Sanyo
128S0386	128S0284		ALL		Kemet alt to Sanyo
128S0397	128S0325		ALL		Kemet alt to Sanyo
377S00011	377S0184		ALL		Infineon alt to Infineon
377S0155	377S0184		ALL		On Semi alt to Infineon
155S0914	155S0897		ALL		Panasonic alt to TDK
371S0558	371S0713		ALL		ST Micro alt to Diodes
128S0436	128S0392		ALL		Kemet alt to Sanyo
128S0445	128S0392		ALL		Panasonic alt to Sanyo
353S00034	353S2220		ALL		Pericom alt to Fairchild
311S00014	311S0515		ALL		Diodes alt to NXP
311S00008	311S0271		ALL		Diodes alt to NXP
197S0479	197S0478		ALL		Epson alt to NDK
311S00013	311S0508		ALL		Diodes alt to NXP
376S00014	376S0761		ALL		Toshiba alt to Vishay
371S00019	371S0463		ALL		Rohm alt to Rohm
371S00018	371S0619		ALL		Rohm alt to Rohm
311S00015	311S0450		ALL		Diodes alt to NXP
371S00017	371S0749		ALL		Diodes alt to Onsemi
353S00107	353S3239	ANY	ALL		Onsemi alt to Intersil
107S00024	107S0226		ALL		Yageo alt to Cyntec
372S0186	372S0185		ALL		NXP alt to Diodes
353S00231	353S3987		ALL		NXP alt to TI
353S00135	353S2220		ALL		Onsemi alt to Fairchild
353S00133	353S2741		ALL		Onsemi alt to TI
131S00040	131S00041		ALL		Murata alt to Taiyo Yuden
107S00015	107S00011		ALL		TFT alt to Cyntec
107S00031	107S00032		ALL		TFT alt to Cyntec
107S00029	107S00030		ALL		TFT alt to Cyntec

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SYNC_MASTER=J14 SYNC_DATE=09/04/2013

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Shield Cans

SH0451 (SM) — SHLD-J44-MLB — USB Cage

SH0450 (SM) — SHIELD-FENCE-MLB-T29-X304 — TBT Cage

Mounting Holes & Slots

OMIT ZT0411 (4P5R2P3-3P5B) — ABOVE GUMSTICK CARD IN MIDDLE OF BOARD (998-1195)

OMIT ZT0413 (6.19X4.60-SNOWMAN) — SNOWMAN-SHAPED SLOT AT LEFT OF MEMORY BANK (998-5879)

OMIT ZT0414 (6.19X4.60-SNOWMAN) — SNOWMAN-SHAPED SLOT AT RIGHT OF MEMORY BANK (998-5879)

TH0400 (TH-NSP, SL-1.1X0.5-1.4X0.8) — Upper TBT can Ground slot (862-0118)

TH0403 (TH-NSP, SL-1.1X0.5-1.4X0.8) — Lower TBT can Ground slot (862-0118)

TH0404 (TH-NSP, SL-1.1X0.45-1.4X0.75) — USB can Ground slot (998-3975)

TH0405 (TH-NSP, SL-1.1X0.45-1.4X0.75) — USB can Ground slot (998-3975)

Memory Shield CAN (806-00037)

SH0452 (SM, SHLD-FENCE-MLB-DRAM-X304)

Rubber Mount Standoffs (860-1448)

SH0460 (2.90D1.2ID-1.35H-SM)
SH0461 (2.90D1.2ID-1.35H-SM)
SH0462 (2.90D1.2ID-1.35H-SM)
SH0465 (2.90D1.2ID-1.35H-SM)
SH0464 (2.90D1.2ID-1.35H-SM)
SH0463 (2.90D1.2ID-1.35H-SM)
SH0466 (2.90D1.2ID-1.35H-SM)
SH0467 (2.90D1.2ID-1.35H-SM)
SH0468 (2.90D1.2ID-1.35H-SM)
SH0469 (2.90D1.2ID-1.35H-SM)

THERMAL MODULE STANDOFF (860-00165)

SH0420 (4.50D1.85ID-1.78H-SM)
SH0421 (4.50D1.85ID-1.78H-SM)
SH0426 (4.50D1.85ID-1.78H-SM)
SH0427 (4.50D1.85ID-1.78H-SM)

SSD STANDOFF (860-00164)

SH0440 (5.00D2.0H)

FAN STANDOFF (860-00183)

SH0441 (STDOFF-4.5ID1.73H-SM)

POGO PINS (870-00607)

SH0435 & SH0436 removed.

SH0432 (POGO-2.30D-5.5H-X304)
SH0433 (POGO-2.30D-5.5H-X304)

RIO FLEX BRACKET BOSSES (860-00166)

SH0443 (3.50D1.85ID-2.0H)

IPD FLEX BRACKET BOSSES (860-00166)

SH0471 (3.50D1.85ID-2.0H)

BOM_COST_GROUP=PD PARTS

SYNC_MASTER=LDUNN_J44 SYNC_DATE=01/13/2013

PAGE TITLE: PD Parts

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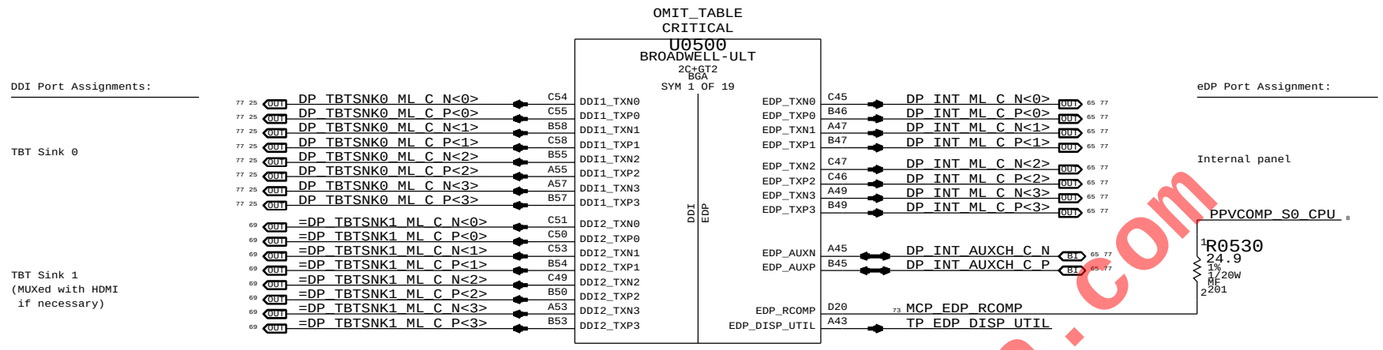
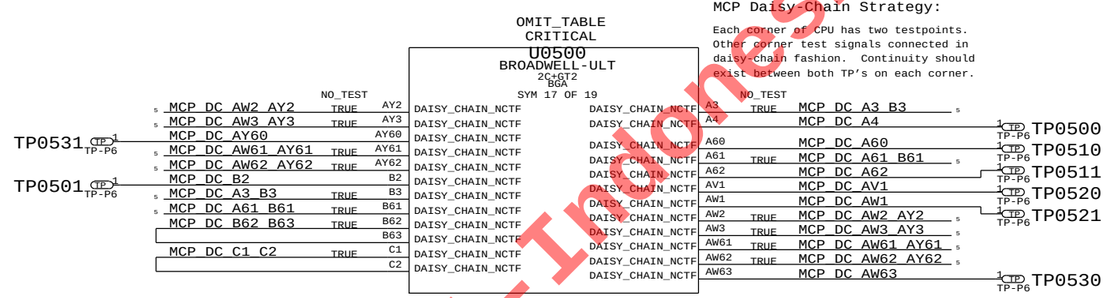
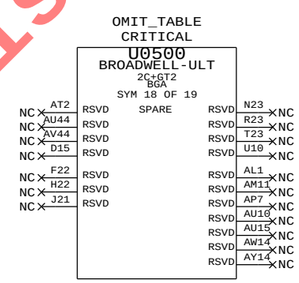




MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.



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BOM_COST_GROUP=CPU

SYNC MASTER=J41	SYNC DATE=10/23/2012
PAGE TITLE: CPU GFX,NCTF,RSVD	
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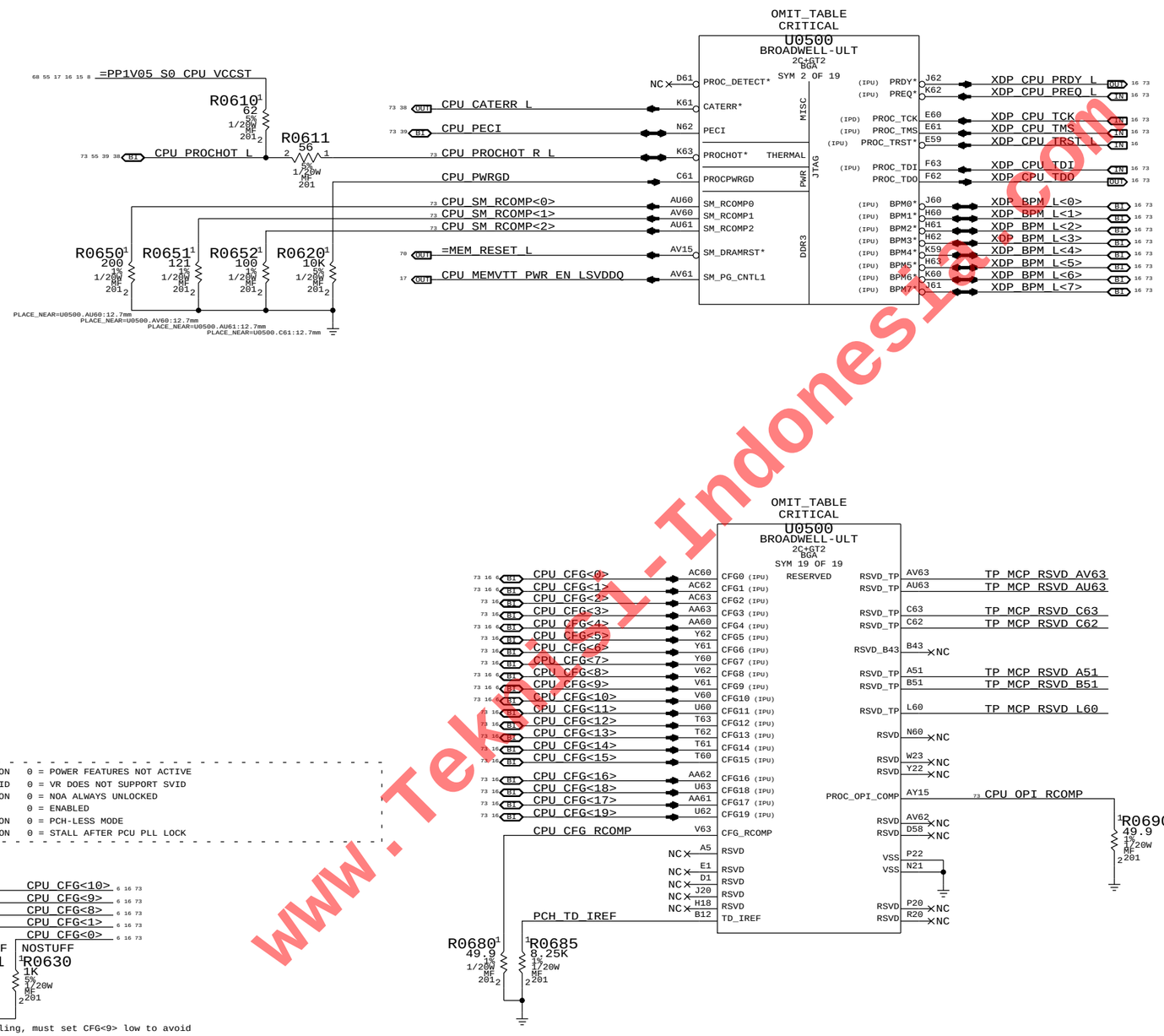

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PAGE TITLE
CPU Misc,JTAG,CFG,RSVD

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CRITICAL
U0500
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MEMORY CHANNEL A

MEM A DQ<0>	AH63	SA_DQ0	SA_CLK0*	AU37	MEM A CLK N<0>
MEM A DQ<1>	AH62	SA_DQ1	SA_CLK0	AV37	MEM A CLK P<0>
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MEM A DQ<3>	AK62	SA_DQ3	SA_CLK1	AY36	MEM A CLK P<1>
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MEM A DQ<11>	AP62	SA_DQ11	SA_CS1*	AR32	MEM A CS L<1>
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MEM A DQ<15>	AP60	SA_DQ15	LPDDR3 CAB3 SA_RAS*	AY34	=MEM A RAS L
MEM A DQ<16>	AP58	SA_DQ16	CAB2 SA_WE*	AW34	=MEM A WE L
MEM A DQ<17>	AR58	SA_DQ17	CAB1 SA_CAS*	AU34	=MEM A CAS L
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MEMORY CHANNEL B

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SYNC MASTER=J41 SYNC DATE=10/23/2013

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CPU LPDDR3 Interfaces

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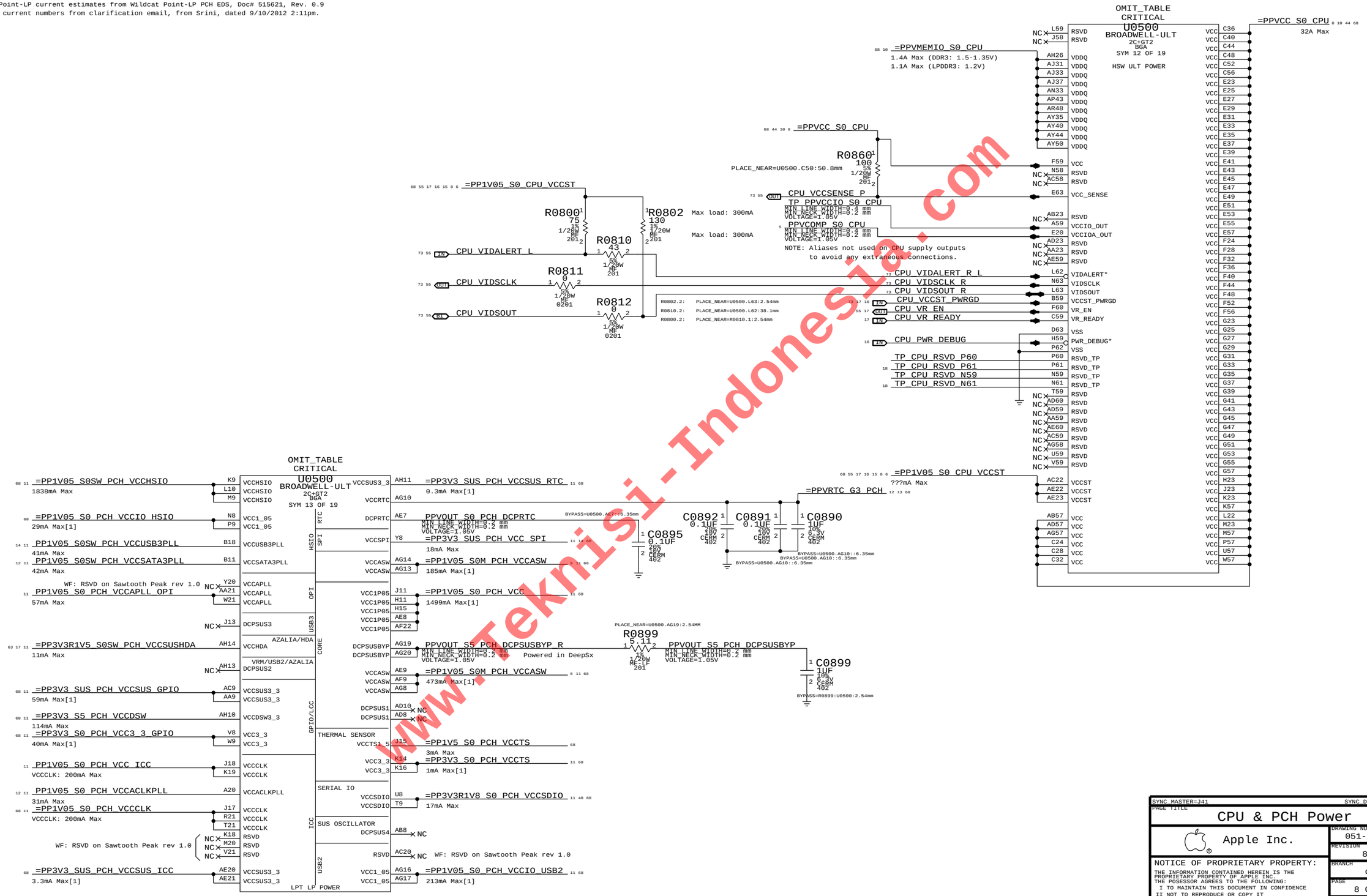
BDW-ULT current estimates from Broadwell Mobile ULT Processor EDS vol.1 Doc# 514405, Rev.: 0.9v1
Wildcat Point-LP current estimates from Wildcat Point-LP PCH EDS, Doc# 515621, Rev. 0.9
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



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CPU & PCH Power

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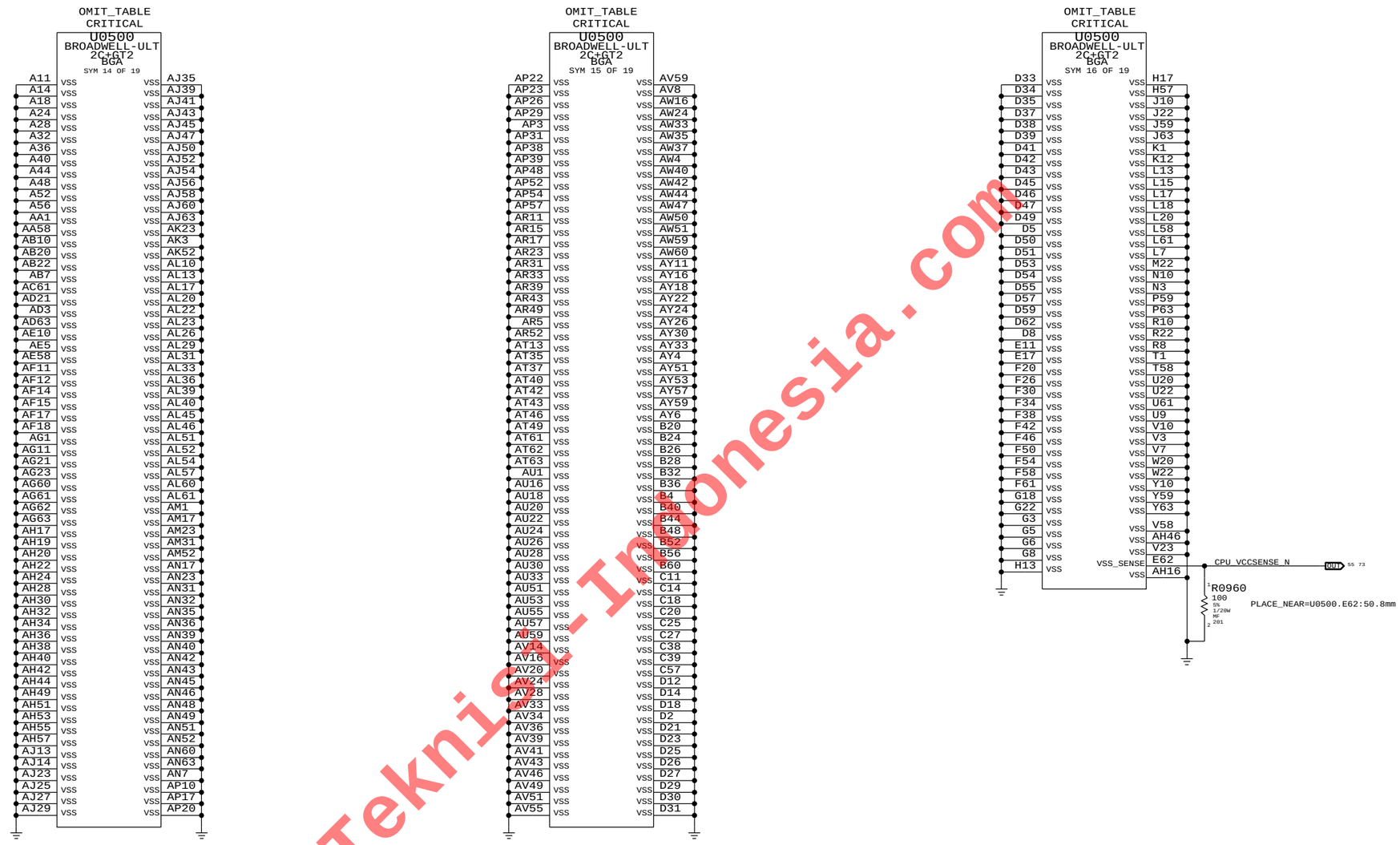

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PAGE TITLE
CPU & PCH Grounds

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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 22uF 0603 stuff, 80x 22uF 0603 nostuff

68 44 8 =PPVCC_S0_CPU

CRITICAL C1000 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1001 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1002 12PF 2% 50V C0G-CERM 0402
CRITICAL C1003 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1004 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1008 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1009 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1010 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1011 12PF 2% 50V C0G-CERM 0402
CRITICAL C1012 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1014 12PF 2% 50V C0G-CERM 0402
CRITICAL C105A 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C105B 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C105C 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C105D 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C105E 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C105F 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1018 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1019 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1020 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1021 12PF 2% 50V C0G-CERM 0402
CRITICAL C1030 12PF 2% 50V C0G-CERM 0402
CRITICAL C104E 12PF 2% 50V C0G-CERM 0402
CRITICAL C104F 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C106D 12PF 2% 50V C0G-CERM 0402
CRITICAL C106E 12PF 2% 50V C0G-CERM 0402
CRITICAL C1070 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1072 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1073 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1074 10UF 20% 4V X6S 0402 OMIT_TABLE
CRITICAL C1075 12PF 2% 50V C0G-CERM 0402
CRITICAL C1077 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1081 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1082 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1083 12PF 2% 50V C0G-CERM 0402
CRITICAL C1084 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1085 12PF 2% 50V C0G-CERM 0402
CRITICAL C1086 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1087 12PF 2% 50V C0G-CERM 0402
CRITICAL C1088 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1089 12PF 2% 50V C0G-CERM 0402
CRITICAL C1090 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1091 12PF 2% 50V C0G-CERM 0402
CRITICAL C1092 12PF 2% 50V C0G-CERM 0402
CRITICAL C1093 12PF 2% 50V C0G-CERM 0402
CRITICAL C1094 12PF 2% 50V C0G-CERM 0402
CRITICAL C1095 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1096 10UF 20% 4V X6S 0402 NO STUFF
CRITICAL C1097 12PF 2% 50V C0G-CERM 0402
CRITICAL C1022 10UF 20% 4V X6S 0402 OMIT_TABLE
C1023 12PF 2% 50V C0G-CERM 0402
C1024 12PF 2% 50V C0G-CERM 0402
NO STUFF C1025 10UF 20% 4V X6S 0402
CRITICAL C1026 10UF 20% 4V X6S 0402 OMIT_TABLE
NO STUFF C1027 10UF 20% 4V X6S 0402
NO STUFF C1028 10UF 20% 4V X6S 0402
NO STUFF C1029 10UF 20% 4V X6S 0402
NO STUFF C1032 10UF 20% 4V X6S 0402
C1033 12PF 2% 50V C0G-CERM 0402
CRITICAL C1034 10UF 20% 4V X6S 0402 OMIT_TABLE
C1035 12PF 2% 50V C0G-CERM 0402
C1036 12PF 2% 50V C0G-CERM 0402
C1037 12PF 2% 50V C0G-CERM 0402
C1038 12PF 2% 50V C0G-CERM 0402
NO STUFF C1039 10UF 20% 4V X6S 0402
C1044 12PF 2% 50V C0G-CERM 0402
NO STUFF C1045 10UF 20% 4V X6S 0402
NO STUFF C1046 10UF 20% 4V X6S 0402
NO STUFF C1047 10UF 20% 4V X6S 0402
NO STUFF C1048 10UF 20% 4V X6S 0402
C1049 12PF 2% 50V C0G-CERM 0402
NO STUFF C1056 10UF 20% 4V X6S 0402
NO STUFF C1057 10UF 20% 4V X6S 0402
C1058 12PF 2% 50V C0G-CERM 0402
NO STUFF C1059 10UF 20% 4V X6S 0402
NO STUFF C1062 10UF 20% 4V X6S 0402
NO STUFF C1063 10UF 20% 4V X6S 0402
C1064 12PF 2% 50V C0G-CERM 0402
CRITICAL C1065 10UF 20% 4V X6S 0402 OMIT_TABLE
NO STUFF C1066 10UF 20% 4V X6S 0402
NO STUFF C1067 10UF 20% 4V X6S 0402
C1068 12PF 2% 50V C0G-CERM 0402
C1069 12PF 2% 50V C0G-CERM 0402
NO STUFF C1098 10UF 20% 4V X6S 0402
C1099 12PF 2% 50V C0G-CERM 0402
NO STUFF C109A 10UF 20% 4V X6S 0402
NO STUFF C109B 10UF 20% 4V X6S 0402
C109C 12PF 2% 50V C0G-CERM 0402
NO STUFF C109D 10UF 20% 4V X6S 0402
C109E 12PF 2% 50V C0G-CERM 0402
NO STUFF C109F 10UF 20% 4V X6S 0402
C108A 12PF 2% 50V C0G-CERM 0402
C108B 12PF 2% 50V C0G-CERM 0402
NO STUFF C108C 10UF 20% 4V X6S 0402
NO STUFF C108D 10UF 20% 4V X6S 0402
NO STUFF C108E 10UF 20% 4V X6S 0402
C108F 12PF 2% 50V C0G-CERM 0402
NO STUFF C107A 10UF 20% 4V X6S 0402
C107B 12PF 2% 50V C0G-CERM 0402

CRITICAL C1031 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0942	18	CAP,CER,10UF,20%,4V,X6S,HRZTL,0402		CRITICAL	

C1000,C1004,C1008,C1012,C1018,C1019,C1020,C1022,C1026,C1034,C1065,C1070,C1074,C105A,C105C,C105D,C104F,C105F

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

68 8 =PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402-LF
C1041 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

Added 2 extra 2.2uF per Harris Beach v0.9 schematic

C1050 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1051 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1052 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1053 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1054 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1055 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1079 12PF 5% 25V NP0-C0G 0201
C1080 12PF 5% 25V NP0-C0G 0201

C1060 270UF 20% 2V TANT CASE-B2-SM
NO STUFF C1061 270UF 20% 2V TANT CASE-B2-SM

1x Bulk nostuff, Harris Beach has 2x nostuff

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	6	CAP,CER,10UF,20%,6.3V,HRZTL,0402		CRITICAL	

C1050,C1051,C1052,C1053,C1054,C1055

CPU VCC Decoupling

NOTE: 38X capacitors are STUFFED and have been changed to 12pF for Noise Floor Reasons (Radar # 17754026).

BOM_COST_GROUP=CPU

SYNC_MASTER=J41 SYNC_DATE=10/23/2012
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 10 OF 120
SHEET: 10 OF 82

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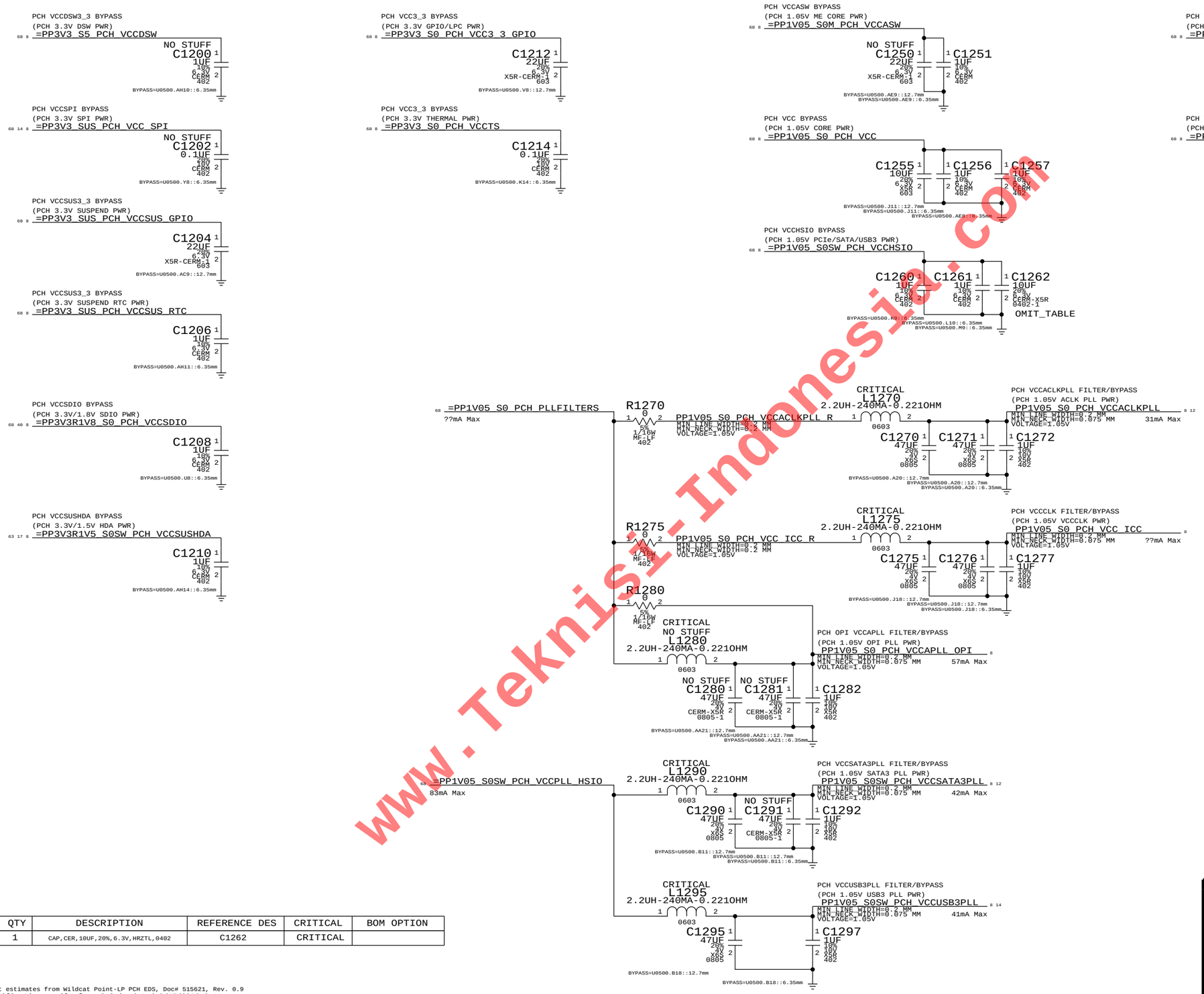

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	1	CAP,CER,10UF,20%,6.3V,HRZTL,0402	C1262	CRITICAL	

Wildcat Point-LP current estimates from Wildcat Point-LP PCH EDS, Doc# 515621, Rev. 0.9
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE: PCH Decoupling

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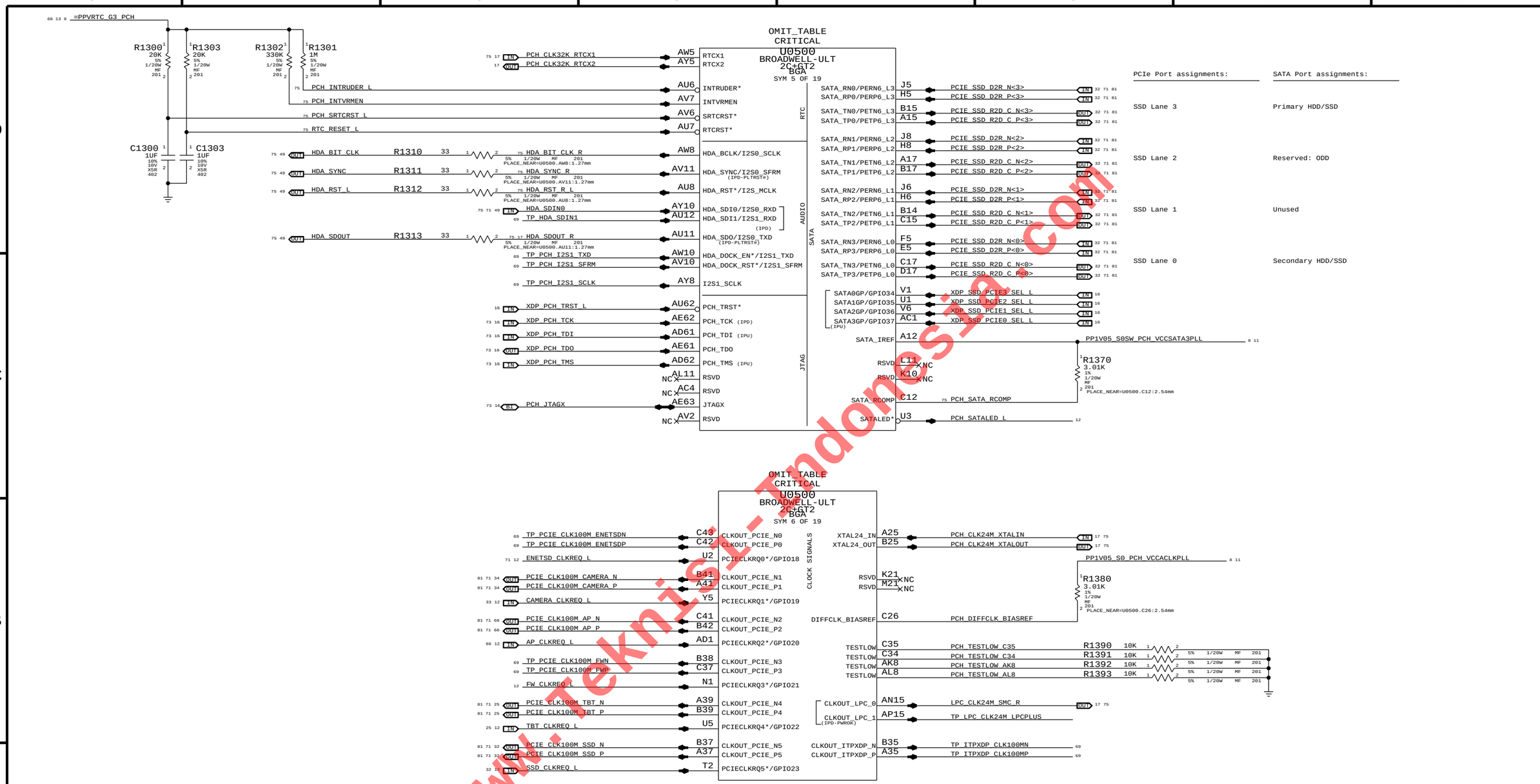

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SYNC MASTER=J41 SYNC DATE=12/17/2012

PAGE TITLE

PCH Audio/JTAG/SATA/CLK

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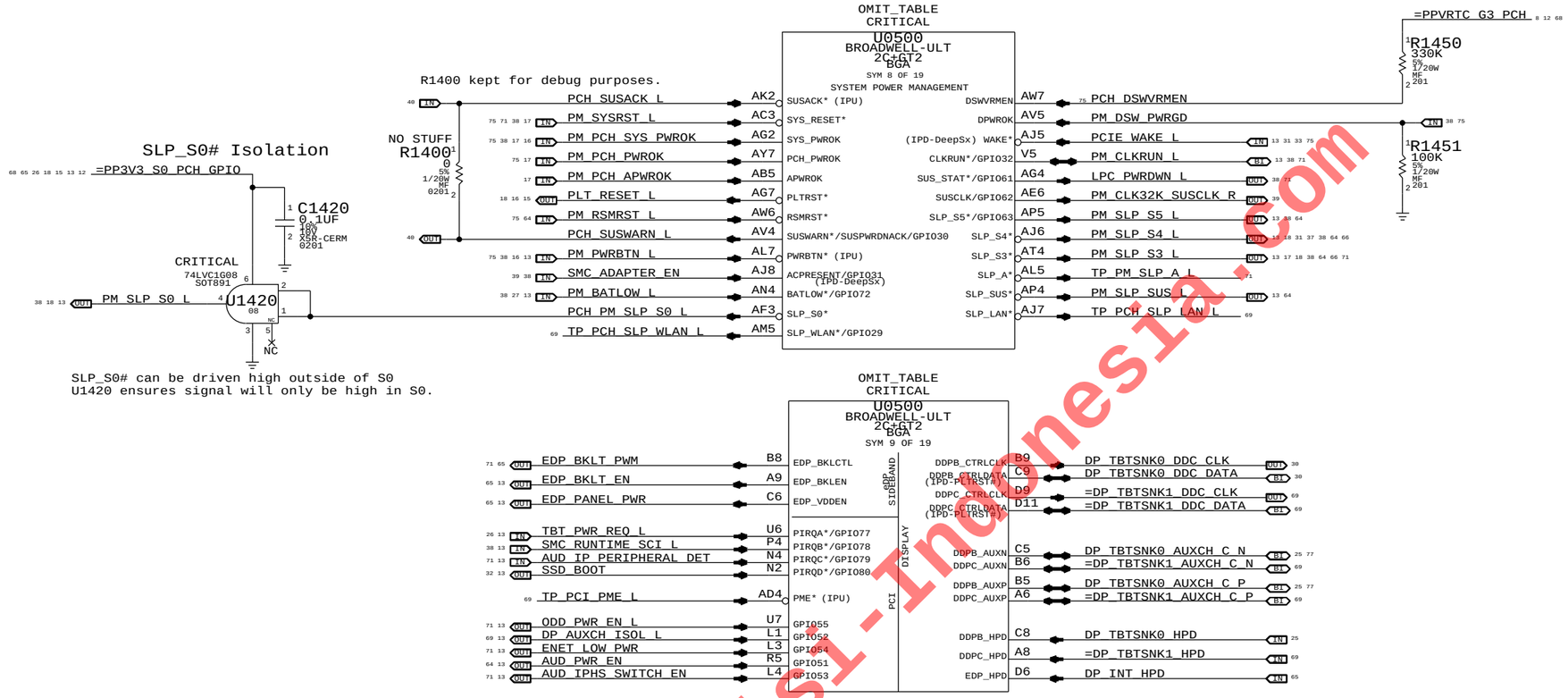

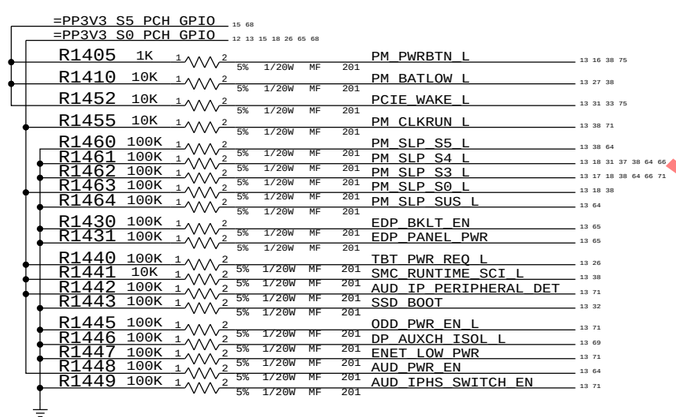

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BOM_COST_GROUP=CPU

SYNC_MASTER=J41 SYNC_DATE=02/21/2013

PAGE TITLE: PCH PM/PCI/GFX

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REVISION: 8.0.0

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PAGE: 14 OF 120

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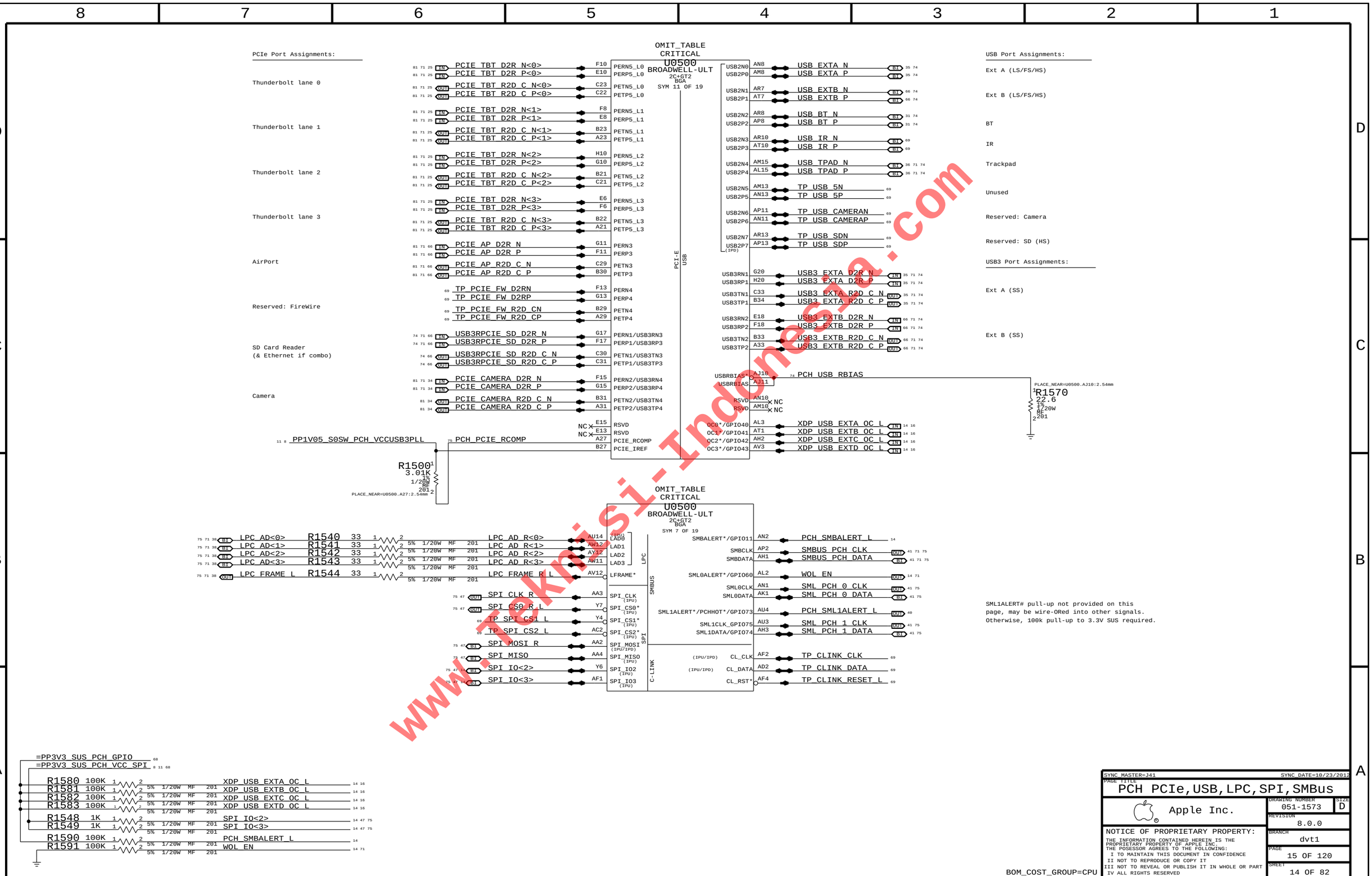

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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

=PP3V3_S0_PCH_GPIO

RAMCFG3:H R1631 100K 5% 1/20W MF 201
RAMCFG2:H R1636 100K 5% 1/20W MF 201
RAMCFG1:H R1635 100K 5% 1/20W MF 201
RAMCFG0:H R1611 100K 5% 1/20W MF 201

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

GPIO12:
CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

=TBT_GO2SX_BIDIR — D1600 BAT54XV2T1 SOD-523

R1600 1M 5% 1/20W MF 201

PLT_RESET_L — R1621 100K 5% 1/20W MF 201

TPAD_SPI_INT_GPIO28_L — R1681 0 5% 1/20W MF 0201
TPAD_SPI_INT_L
R1682 0 5% 1/20W MF 0201 — TPAD_SPI_INT_GPIO46_L

R1639 100K 5% 1/20W MF 201
R1680 100K 5% 1/20W MF 201

=PP3V3_S0_PCH_GPIO — R1641 1K 5% 1/20W MF 201

OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT 2C+GT2 BGA
SYM 10 OF 19

Pin	Signal	Net
P1	BMBUSY*/GPIO76	XDP_PCH_GPIO76
AU2	GPIO8	XDP_MLB_RAMCFG0
AM7	LAN_PHY_PWR_CTRL/GPIO12	HDMI_TBT_MUX_SEL_GPIO12
AD6	GPIO15 (IPD-RSMRST#)	TP_MEM_VDD_SEL_1V5_L
Y1	GPIO16	XDP_LPCPLUS_GPIO
T3	GPIO17	XDP_PCH_GPIO17
AD5	GPIO24	SD_RESET_L
AN5	GPIO27 (IPD-DeepSx)	SMC_WAKE_SCI_L
AD7	GPIO28	TPAD_SPI_INT_GPIO28_L
AN3	GPIO26	TPAD_USB_IF_EN
AG6	GPIO56	SSD_PWR_EN
AP1	GPIO57	PCH_TBT_PCIE_RESET_L
AL4	GPIO58	HDD_PWR_EN
AT5	GPIO59	XDP_SDCONN_STATE_CHANGE_L
AK4	GPIO44	SD_PWR_EN
AB6	GPIO47	TBT_PWR_EN
U4	GPIO48	XDP_JTAG_ISP_TCK
Y3	GPIO49	XDP_JTAG_ISP_TDI
P3	GPIO50	JTAG_TBT_TMS_PCH
Y2	HSIOPC/GPIO71	PCH_HSIO_PWR_EN
AT3	GPIO13	TPAD_SPI_IF_EN
AH4	GPIO14	XDP_MLB_RAMCFG3
AM4	GPIO25	SPIROM_USE_MLB
AG5	GPIO45	CAMERA_PWR_EN_PCH
AG3	GPIO46	TPAD_SPI_INT_GPIO46_L
AM3	GPIO9	XDP_MLB_RAMCFG1
AM2	GPIO10	XDP_MLB_RAMCFG2
P2	DEVSLP0/GPIO33	SSD_SR_EN_L
C4	SDIO_POWER_EN/GPIO70	AP_S0IX_WAKE_SEL
L2	DEVSLP1/GPIO38	SSD_RESET_L
N5	DEVSLP2/GPIO39	CAM_PCIE_RESET_L
V2	SPKR/GPIO81 (IPD-PLTRST#)	PCH_TCO_TIMER_DISABLE

CPU/MISC

Pin	Signal	Net
D60	THERMTRIP*	PM_THRMTRIP_L
V4	RCIN*/GPIO82	=TBT_CIO_PLUG_EVENT
T4	SERIRQ	LPC_SERIRQ
AW15	PCH_OPI_COMP	PCH_OPI_COMP
AF20	RSVD	NC
AB21	RSVD	NC

=PP1V05_S0_CPU_VCCST — R1650 1K 5% 1/20W MF 201

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

PLACE_NEAR=U0500.AW15:2.54mm — R1655 49.9 1% 1/20W MF 201

GPIO LPIO

Pin	Signal	Net
R6	GSPI0_CS*/GPIO83	PCH_GSPI0_CS_L
L6	GSPI0_CLK/GPIO84	PCH_GSPI0_CLK
N6	GSPI0_MISO/GPIO85 (IPD)	PCH_GSPI0_MISO
L8	GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	PCH_GSPI0_MOSI
R7	GSPI1_CS*/GPIO87	TPAD_SPI_CS_L
L5	GSPI1_CLK/GPIO88	TPAD_SPI_CLK
N7	GSPI1_MISO/GPIO89 (IPD)	TPAD_SPI_MISO
K2	GSPI_MOSI/GPIO90	TPAD_SPI_MOSI
J1	UART0_RXD/GPIO91	AP_S0IX_WAKE_L
K3	UART0_TXD/GPIO92	HDMITBTMUX_FLAG_L
J2	UART0_RTS*/GPIO93	JTAG_ISP_TDO
G1	UART0_CTS*/GPIO94	AP_RESET_L
K4	UART1_RXD/GPIO00	PCH_UART1_RXD
G2	UART1_TXD/GPIO01	PCH_UART1_TXD
J3	UART1_RST*/GPIO02	PCH_UART1_RTS_L
J4	UART1_CTS*/GPIO03	PCH_UART1_CTS_L
F2	I2C0_SDA/GPIO04	PCH_I2C0_SDA
F3	I2C0_SCL/GPIO05	PCH_I2C0_SCL
G4	I2C1_SDA/GPIO06	PCH_I2C1_SDA
F1	I2C1_SCL/GPIO07	PCH_I2C1_SCL
E3	SDIO_CLK/GPIO64	TBT_POC_RESET_L
F4	SDIO_CMD/GPIO65	BT_PWRRST_L
D3	SDIO_D0/GPIO66 (IPD-PLTRST#)	PCH_STRP_TOPBLK_SWP_L
E4	SDIO_D1/GPIO67	ENET_MEDIA_SENSE
C3	SDIO_D2/GPIO68	LCD_IRQ_L
E2	SDIO_D3/GPIO69	LCD_PSR_EN

PLT_RESET_L — R1671 100K 5% 1/20W MF 201

Pull-up on TBT page

Requires connection to SMC via 1K series R

R1694 10K 5% 1/20W MF 201 — PP3V3_S0_EDP_SW

=PP3V3_S5_PCH_GPIO
=PP3V3_S3RS4_PCH_GPIO
=PP3V3_S3SW_SD_RESET
=PP3V3_S3_PCH_GPIO
=PP3V3_S3RS0_CAMPWREN
=PP3V3_S0_PCH_GPIO
=PP3V3_S0RTBTLC_PCH_GPIO

TBTLC for CR, S0 for RR

R1610	100K	XDP_PCH_GPIO76
R1614	100K	XDP_LPCPLUS_GPIO
R1615	100K	XDP_PCH_GPIO17
	SD_ON_MLB	
R1616	100K	SD_RESET_L
R1617	100K	SMC_WAKE_SCI_L
R1618	100K	TPAD_SPI_INT_L
R1619	100K	TPAD_USB_IF_EN
R1620	100K	SSD_PWR_EN
R1622	100K	HDD_PWR_EN
R1623	100K	XDP_SDCONN_STATE_CHANGE_L
R1624	100K	SD_PWR_EN
R1625	100K	TBT_PWR_EN
R1626	100K	XDP_JTAG_ISP_TCK
R1627	100K	XDP_JTAG_ISP_TDI
R1628	100K	JTAG_TBT_TMS_PCH
R1629	100K	PCH_HSIO_PWR_EN
R1630	100K	TPAD_SPI_IF_EN
R1632	100K	SPIROM_USE_MLB
R1633	100K	CAMERA_PWR_EN_PCH
R1637	100K	SSD_SR_EN_L
R1638	100K	AP_S0IX_WAKE_SEL
R1652	10K	LPC_SERIRQ
R1670	100K	JTAG_ISP_TDO
R1691	100K	BT_PWRRST_L
R1693	100K	ENET_MEDIA_SENSE
R1695	100K	LCD_PSR_EN

R1616 should also be stuffed if platform does not use SD card

STUFFED R1632

=PP3V3_S0_PCH_GPIO

PCH_GSPI0_CS_L	R1660	100K
PCH_GSPI0_CLK	R1661	100K
PCH_GSPI0_MISO	R1662	100K
PCH_GSPI0_MOSI	R1663	100K
TPAD_SPI_CS_L	R1664	47K
TPAD_SPI_CLK	R1665	47K
TPAD_SPI_MISO	R1666	47K
TPAD_SPI_MOSI	R1667	47K
AP_S0IX_WAKE_L	R1668	100K
HDMITBTMUX_FLAG_L	R1669	100K
PCH_UART1_RXD	R1672	100K
PCH_UART1_TXD	R1673	100K
PCH_UART1_RTS_L	R1674	100K
PCH_UART1_CTS_L	R1675	100K
PCH_I2C0_SDA	R1676	100K
PCH_I2C0_SCL	R1677	100K
PCH_I2C1_SDA	R1678	100K
PCH_I2C1_SCL	R1679	100K

BOM COST GROUP=CPU

SYNC MASTER=J41 SYNC DATE=01/19/2013
PAGE TITLE: PCH GPIO/MISC/LPIO
Apple Inc.
DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 16 OF 120
SHEET: 15 OF 82

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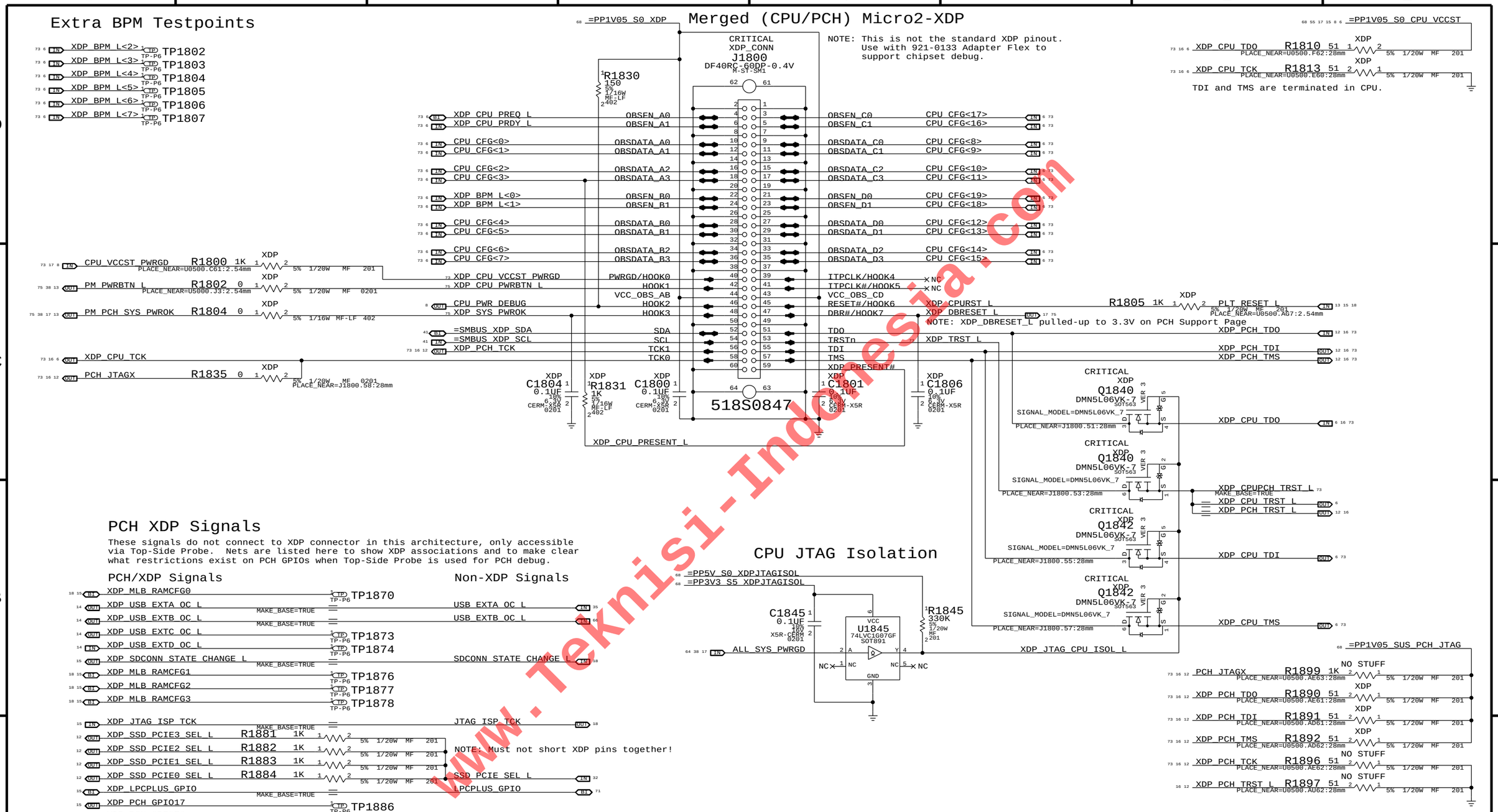

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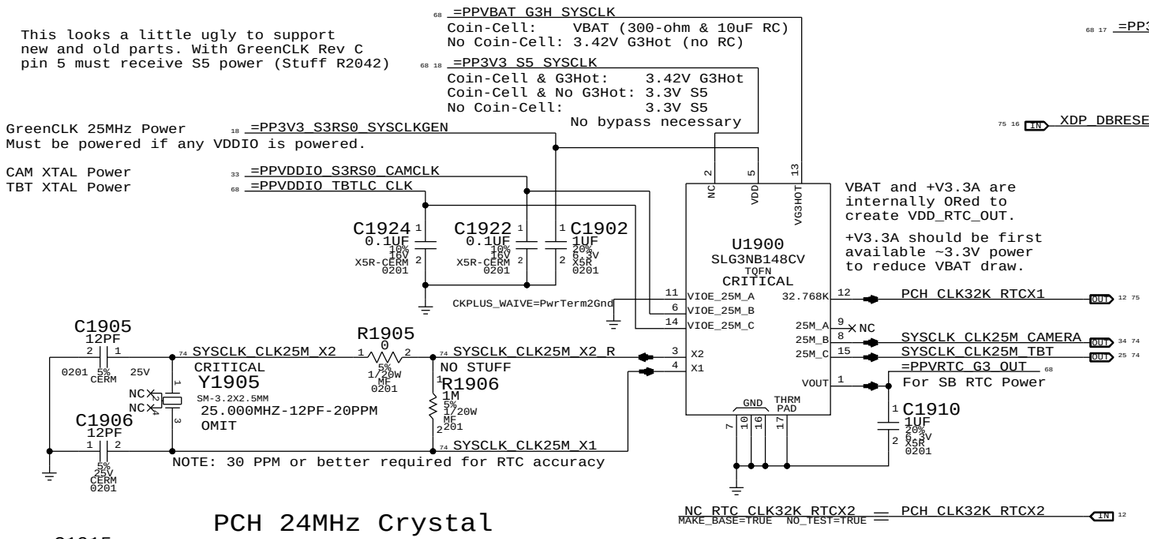
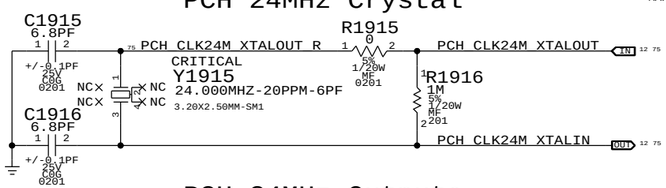
System RTC Power Source & 32kHz / 25MHz Clock Generator

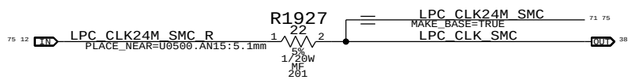
Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal



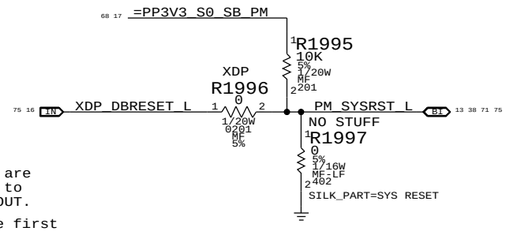
PCH 24MHz Crystal



PCH 24MHz Outputs

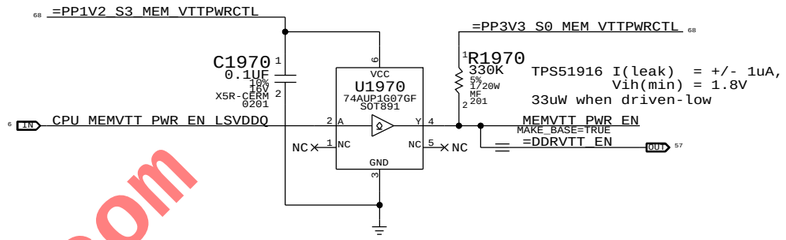


PCH Reset Button

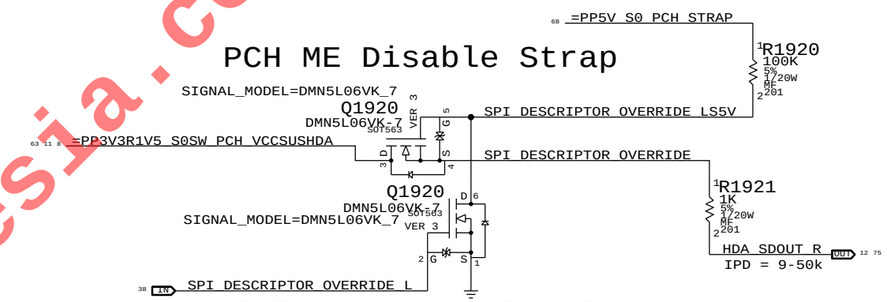


Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

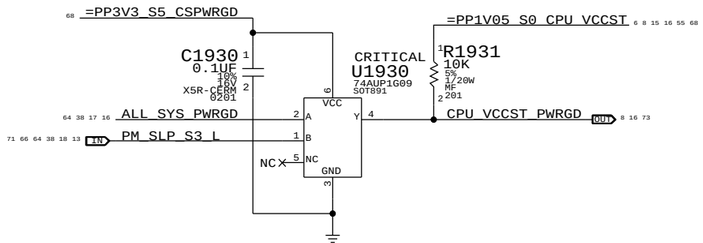


PCH ME Disable Strap

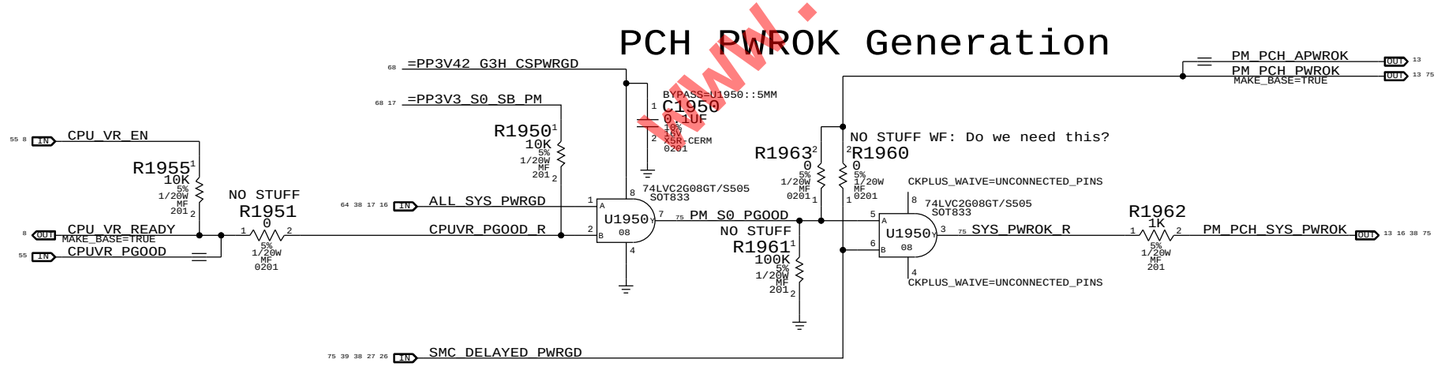


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD



PCH PWROK Generation



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0480	1	XTAL,25MHZ,20PPM,12PF,3.2X2.5X.6MM,85C	Y1905		

BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=J41 SYNC_DATE=01/30/2013

PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 19 OF 120

SHEET: 17 OF 82

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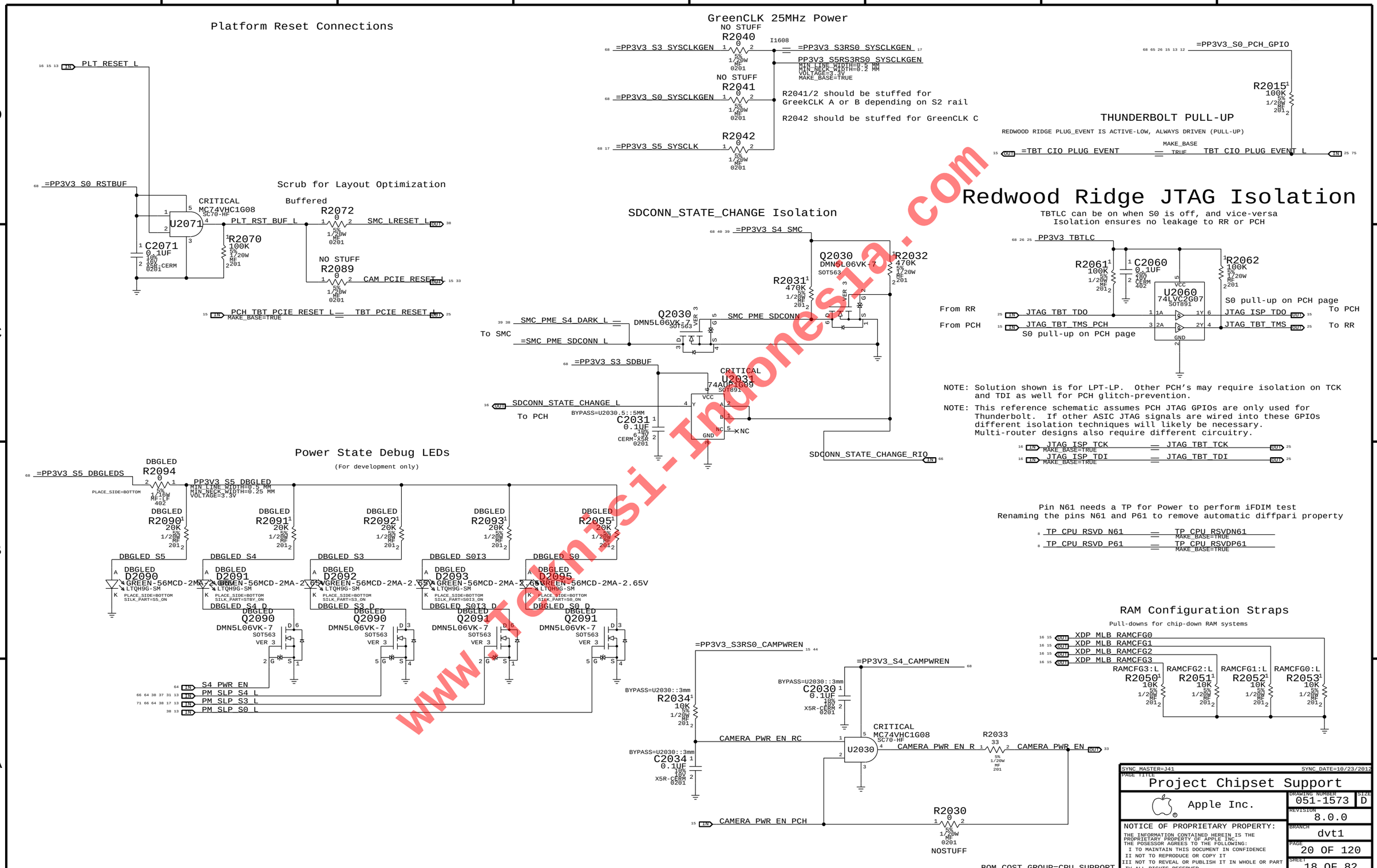

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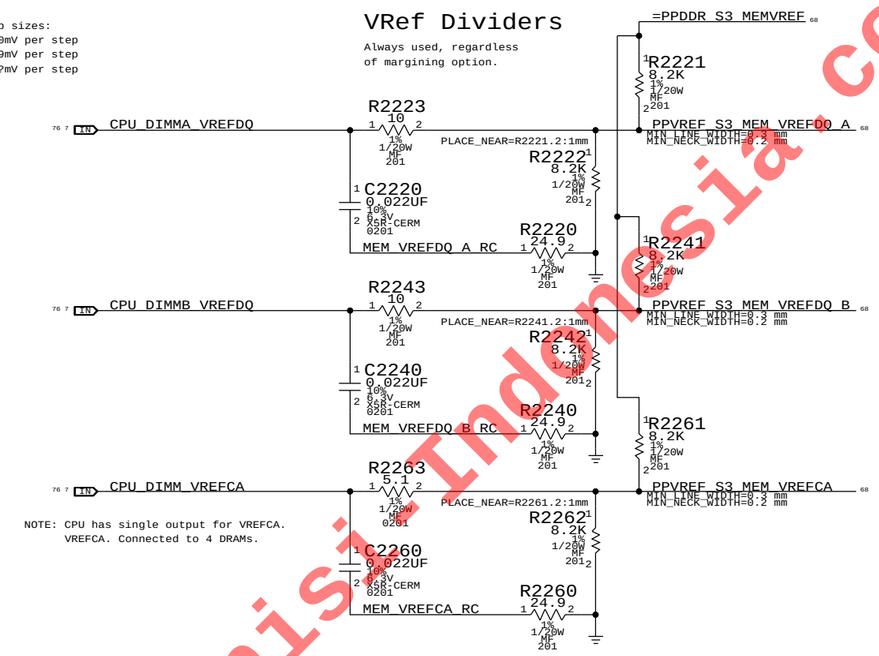
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step



NOTE: CPU has single output for VREFCA.
VREFCA. Connected to 4 DRAMs.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/02/2013

PAGE TITLE
LPDDR3 VREF Margining

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 22 OF 120
SHEET 19 OF 82

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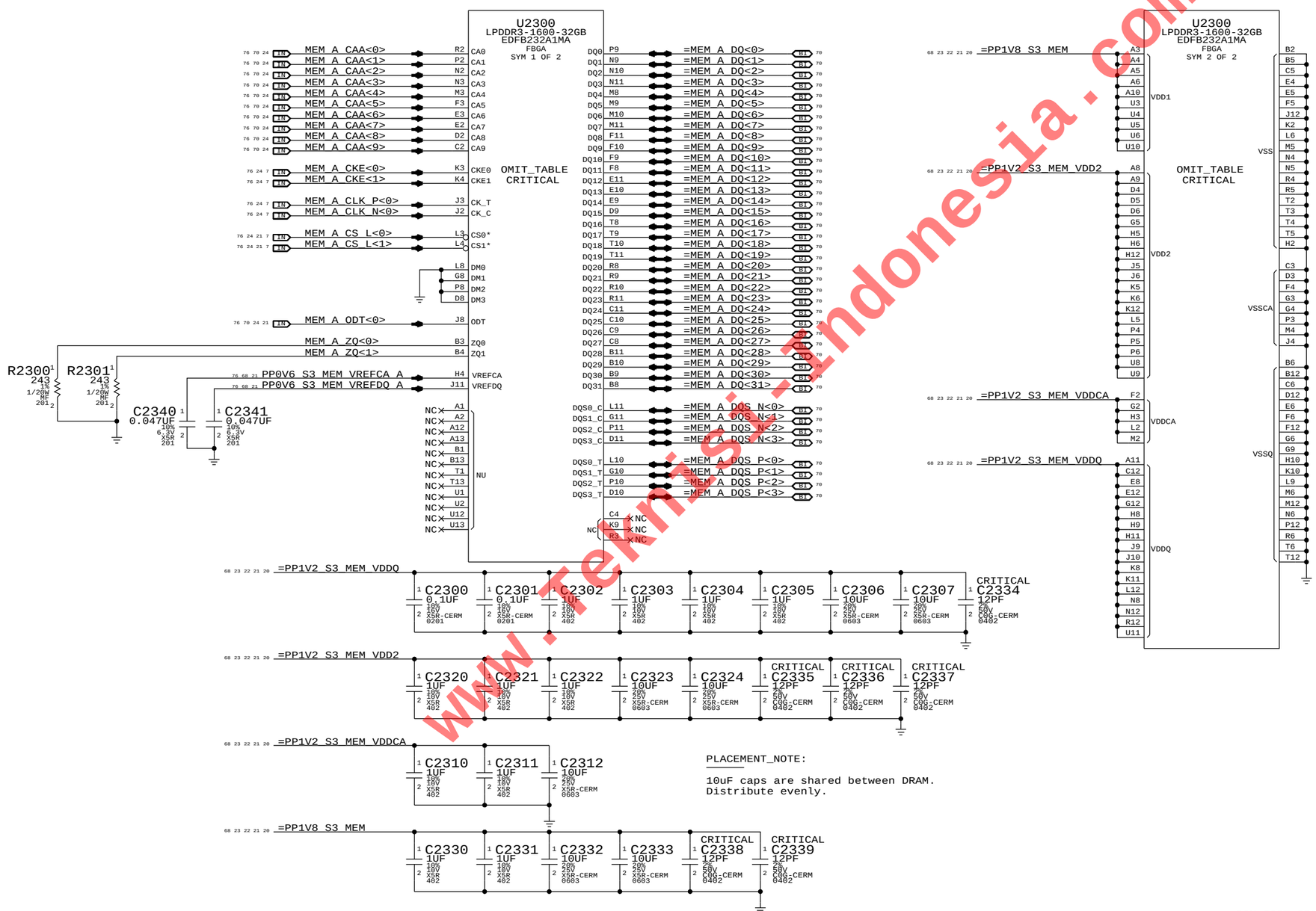
LPDDR3 CHANNEL A (0-31)



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BOM_COST_GROUP=DRAM

SYNC_MASTER=J41_MLB	SYNC_DATE=02/06/2013
PAGE TITLE: LPDDR3 DRAM Channel A (00-31)	
Apple Inc.	DRAWING NUMBER: 051-1573 SIZE: D
	REVISION: 8.0.0
	BRANCH: dvt1
	PAGE: 23 OF 120
	SHEET: 20 OF 82

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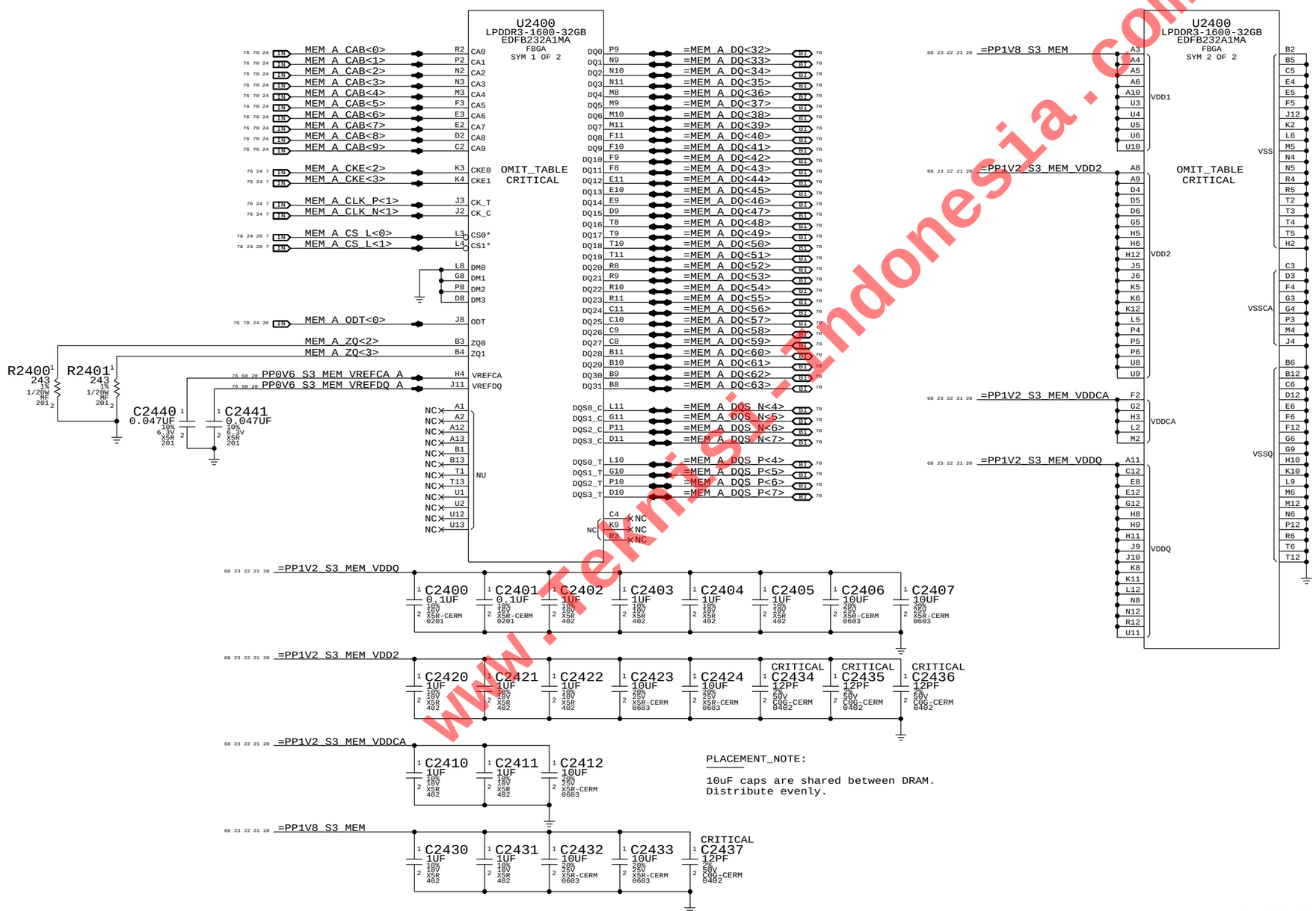
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 24 OF 120
SHEET 21 OF 82

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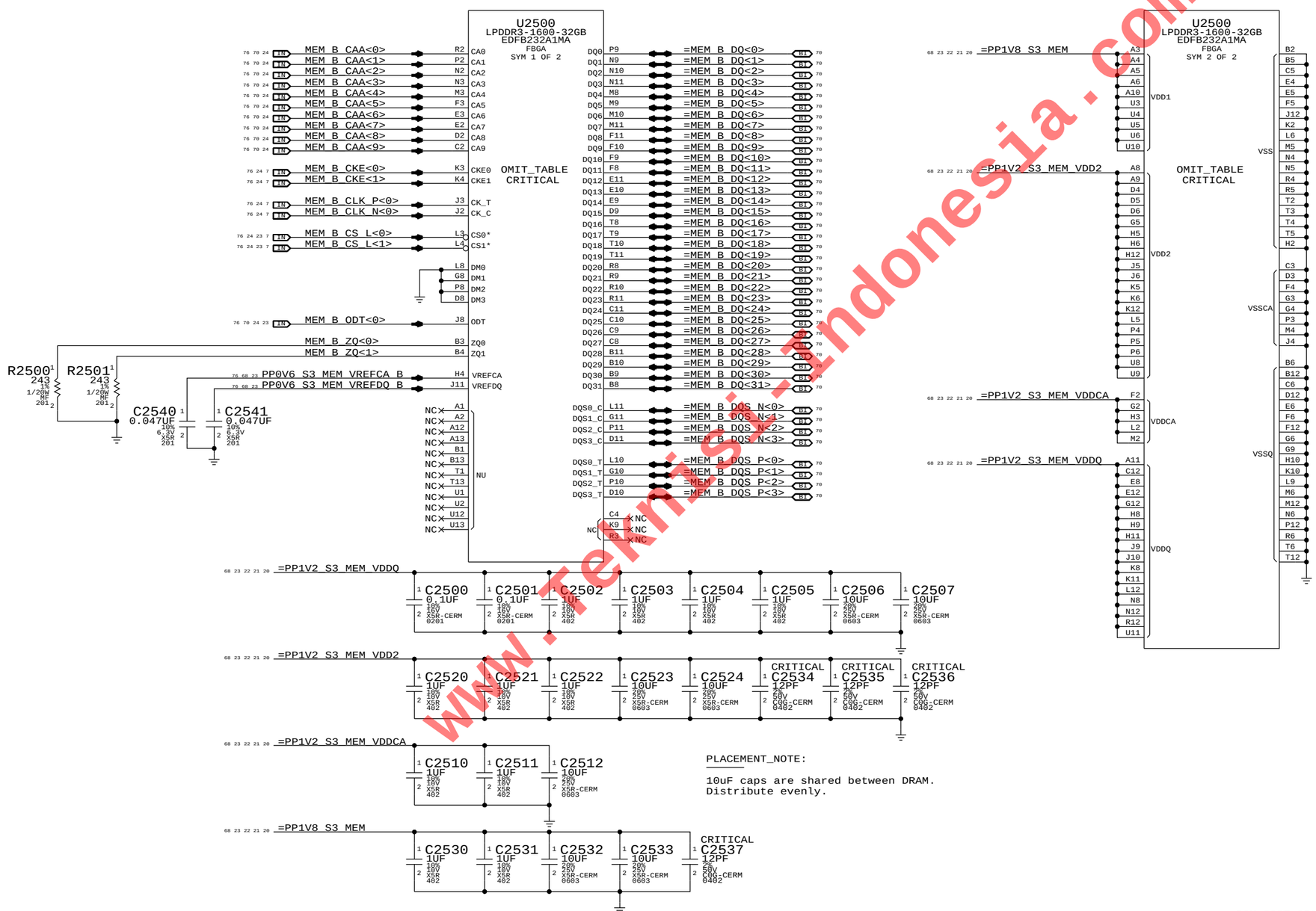
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel B (00-31)

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 25 OF 120
SHEET 22 OF 82

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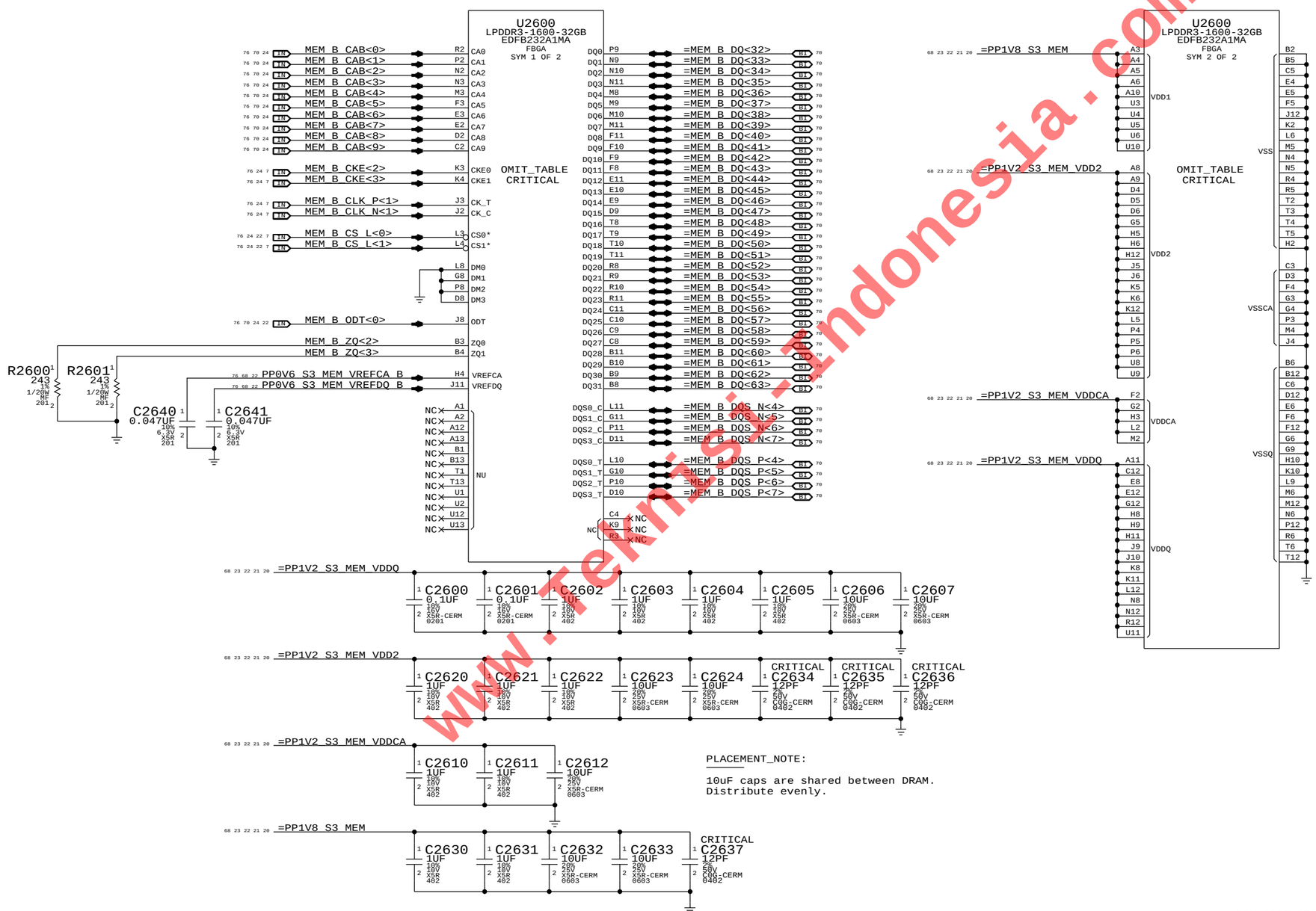
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER 051-1573
SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 26 OF 120
SHEET 23 OF 82

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Intel recommends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

=PP0V6_S0_MEM_VTT_A

MEM_A_CAA<9>	R2700	56	1% 1/20W 201 MF
MEM_A_CAA<8>	R2701	56	1% 1/20W 201 MF
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MEM_A_ODT<0>	R2730	82	1% 1/20W 201 MF

C2700 0.47UF 20% 4V CERM-X5R-1 201
C2730 12PF 5% 50V NPO-C0G 0201
C2701 0.47UF 20% 4V CERM-X5R-1 201
C2702 0.47UF 20% 4V CERM-X5R-1 201
C2703 0.47UF 20% 4V CERM-X5R-1 201
C2704 0.47UF 20% 4V CERM-X5R-1 201
C2705 0.47UF 20% 4V CERM-X5R-1 201
C2706 0.47UF 20% 4V CERM-X5R-1 201
C2707 0.47UF 20% 4V CERM-X5R-1 201
C2708 0.47UF 20% 4V CERM-X5R-1 201
C2709 0.47UF 20% 4V CERM-X5R-1 201
CRITICAL
C2720 22UF 20% 6.3V X6S-CERM-1 603

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MEM_B_CKE<3>	R2762	82	1% 1/20W 201 MF
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C2710 0.47UF 20% 4V CERM-X5R-1 201
C2731 12PF 5% 50V NPO-C0G 0201
C2711 0.47UF 20% 4V CERM-X5R-1 201
C2712 0.47UF 20% 4V CERM-X5R-1 201
C2713 0.47UF 20% 4V CERM-X5R-1 201
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C2716 0.47UF 20% 4V CERM-X5R-1 201
C2717 0.47UF 20% 4V CERM-X5R-1 201
C2718 0.47UF 20% 4V CERM-X5R-1 201
C2719 0.47UF 20% 4V CERM-X5R-1 201
CRITICAL
C2740 22UF 20% 6.3V X6S-CERM-1 603

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BOM_COST_GROUP=DRAM

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 27 OF 120

SHEET: 24 OF 82

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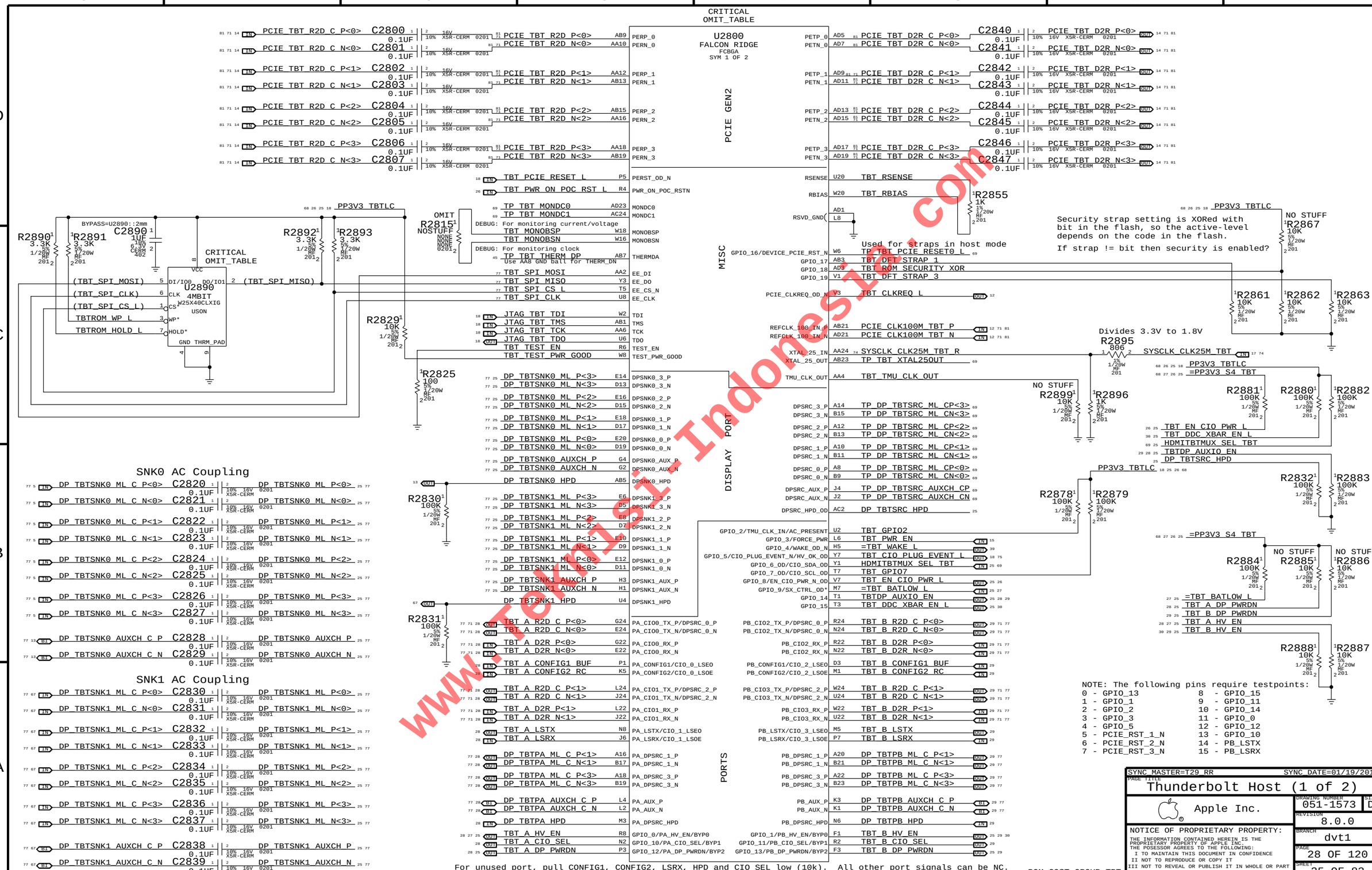

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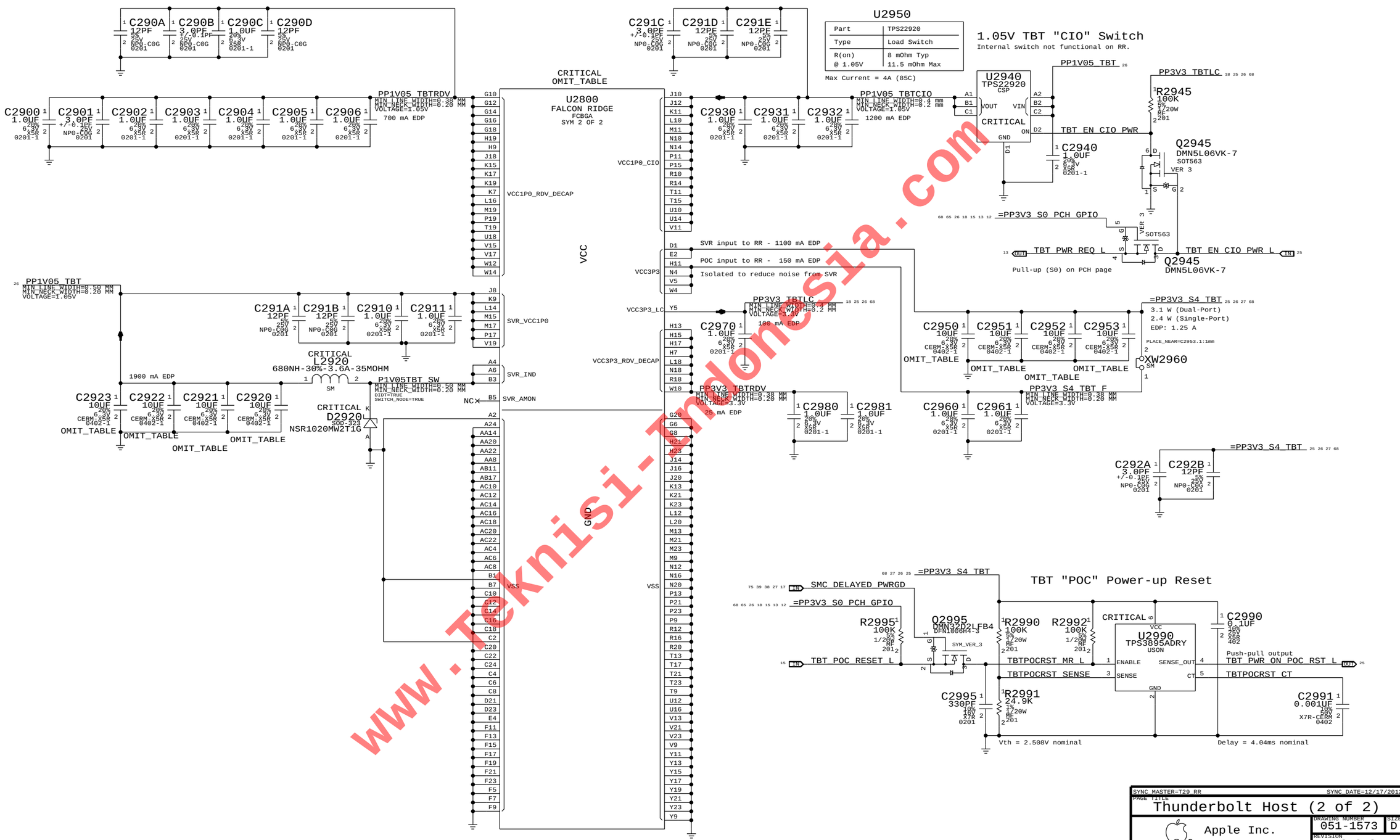

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	8	CAP,CER,10UF,20%,6.3V,HRZTL,0402		CRITICAL	

C2920,C2921,C2922,C2923,C2950,C2951,C2952,C2953

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

BOM_COST_GROUP=TBT

SYNC MASTER=T29_RR SYNC_DATE=12/17/2012

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 29 OF 120

SHEET 26 OF 82

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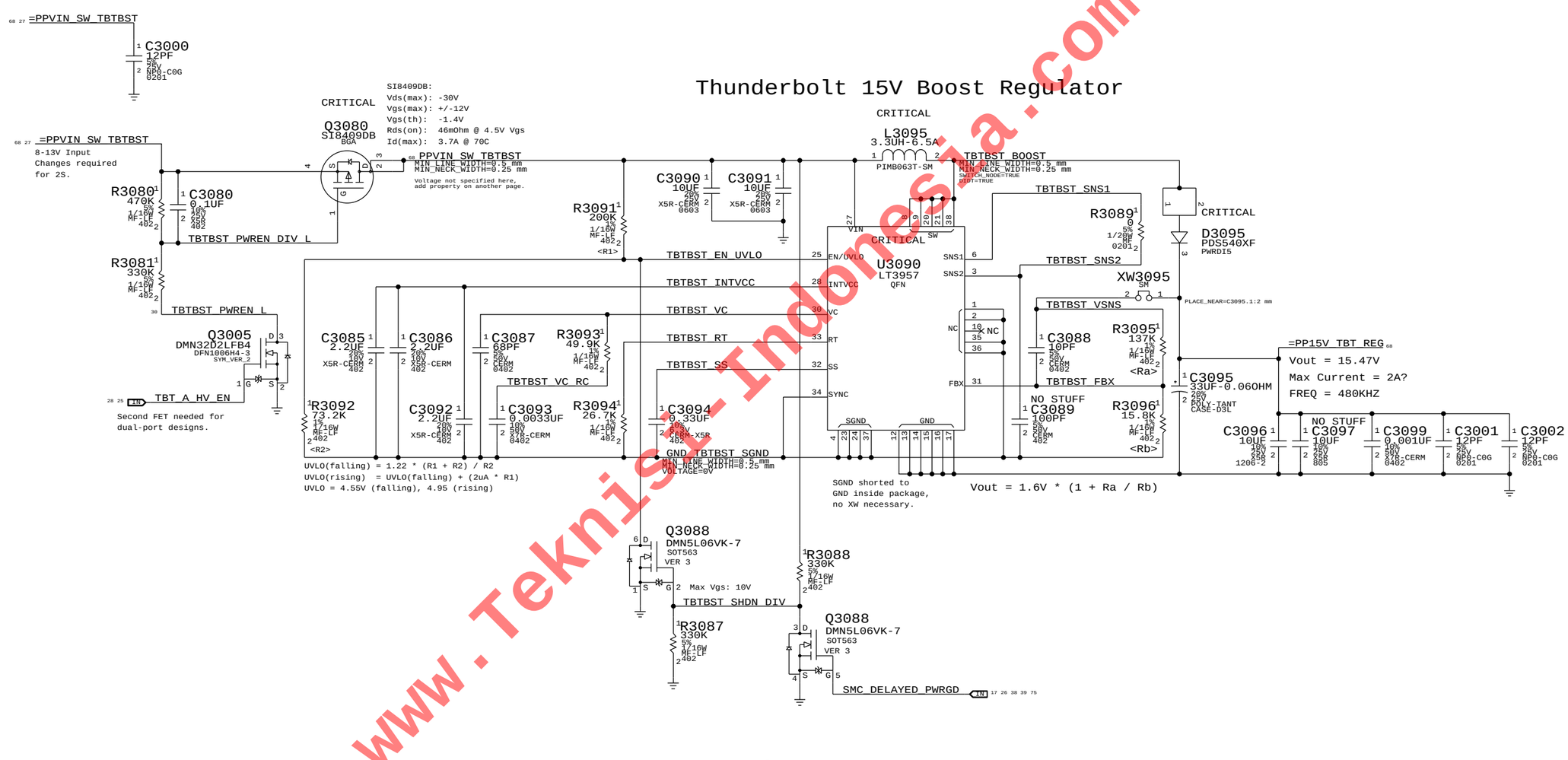
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

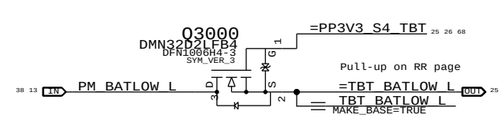
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator



BATLOW# Isolation



BOM_COST_GROUP=TBT

SYNC_MASTER=T29_RR SYNC_DATE=11/19/2013

PAGE TITLE: Thunderbolt Mobile Support

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 30 OF 120

SHEET: 27 OF 82

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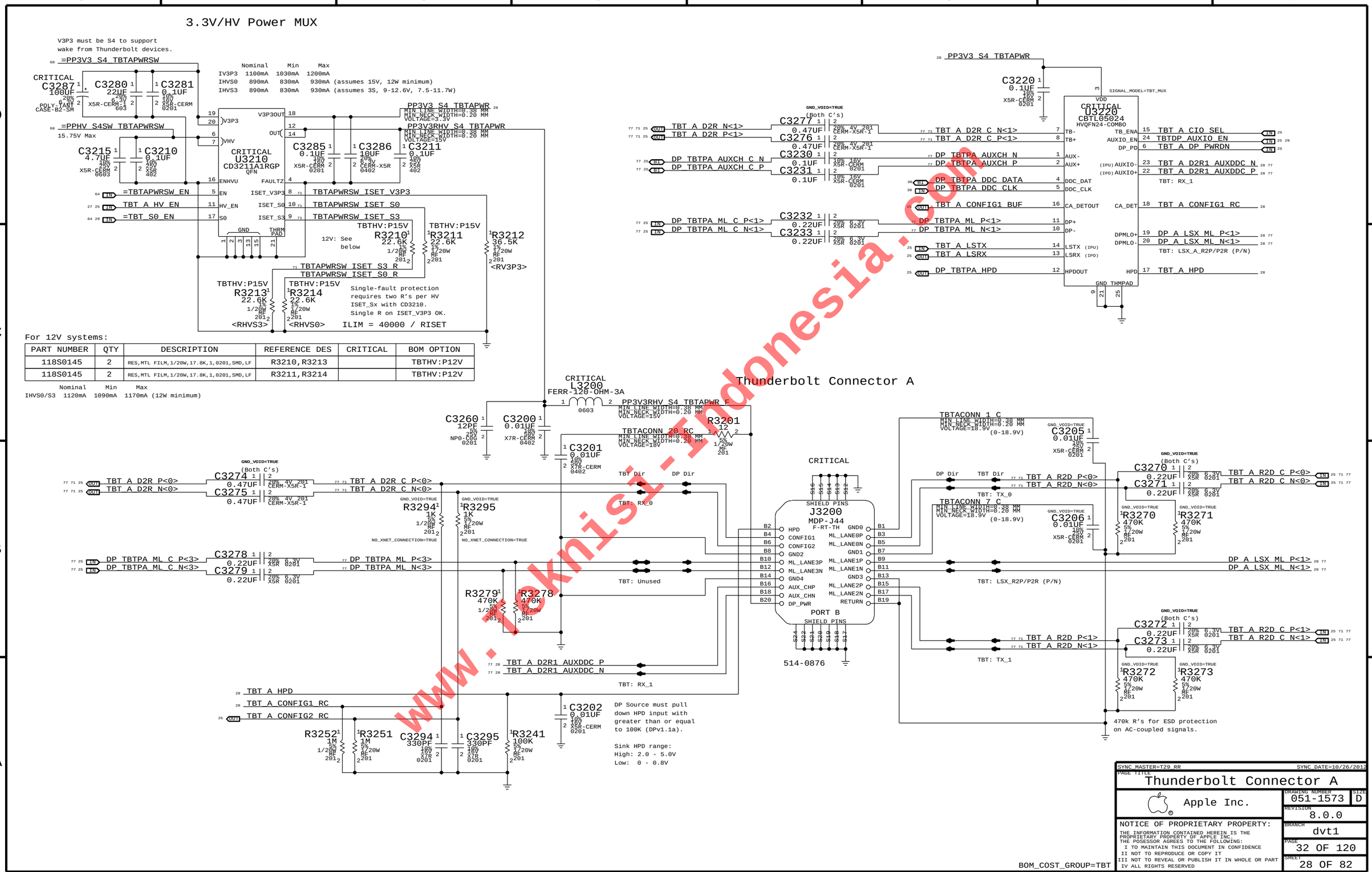

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

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SYNC MASTER=T29_RR SYNC DATE=10/26/2012

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 32 OF 120

SHEET: 28 OF 82

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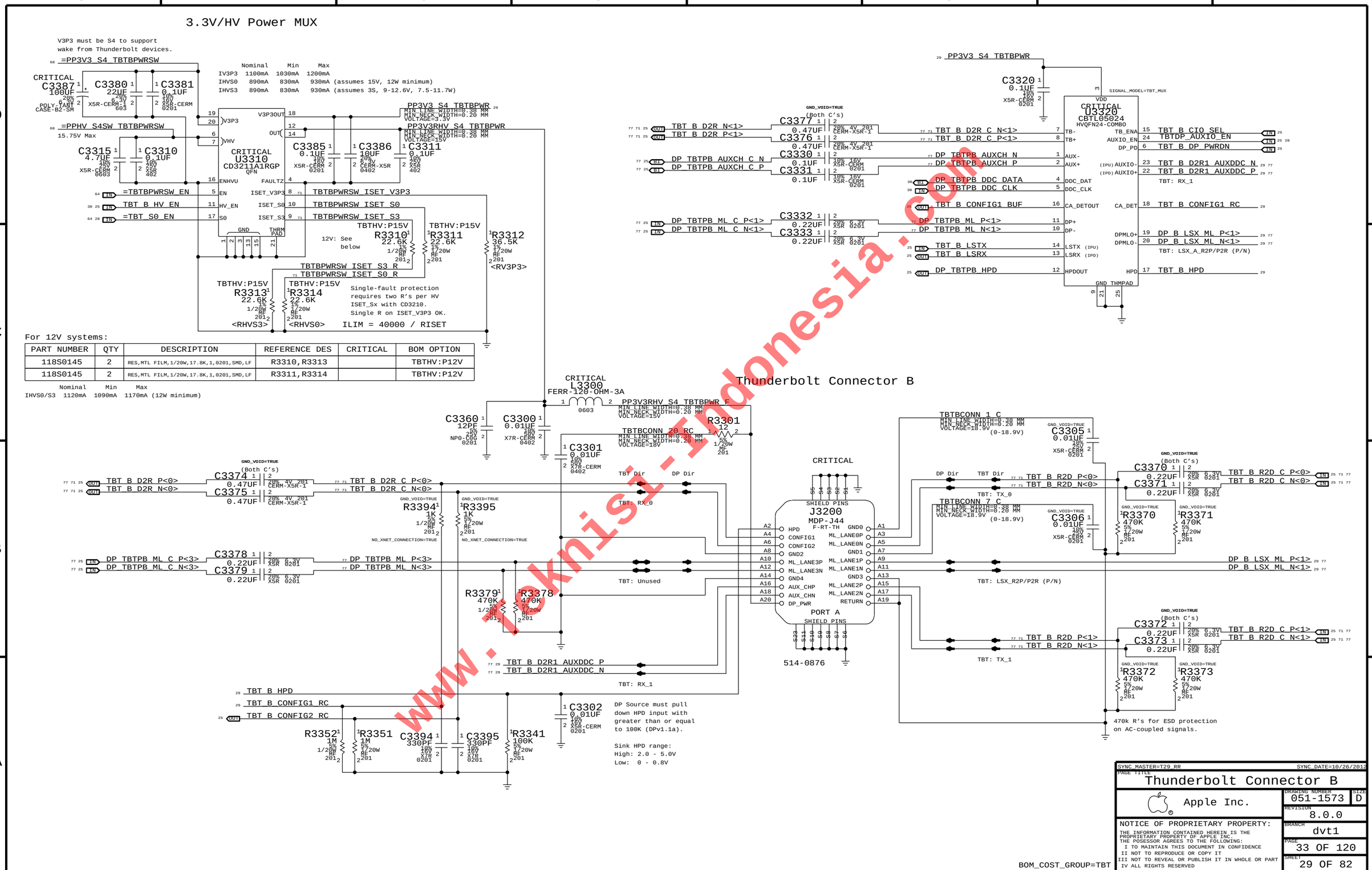

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

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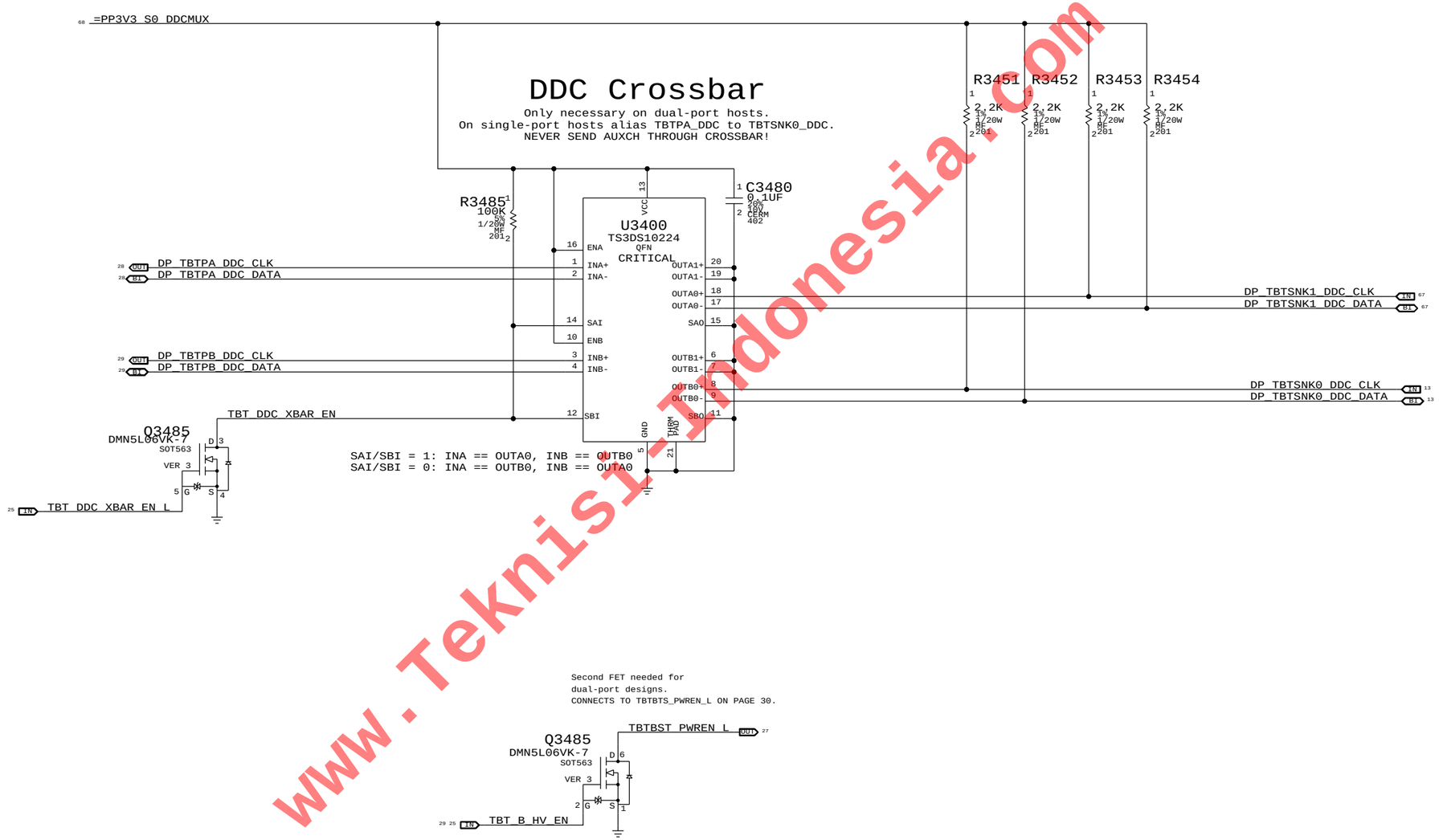
DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK
pull-ups are unstuffed.



Second FET needed for
dual-port designs.
CONNECTS TO TBTBTS_PWREN_L ON PAGE 30.

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BOM_COST_GROUP=TBT

SYNC MASTER=J14	SYNC DATE=10/23/2012
PAGE TITLE: DDC Crossbar	
Apple Inc.	DRAWING NUMBER: 051-1573 SIZE: D
	REVISION: 8.0.0
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	SHEET: 30 OF 82

SYNC MASTER=J41 SYNC DATE=11/01/2012

PAGE TITLE

Wireless Support

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 35 OF 120

SHEET 31 OF 82

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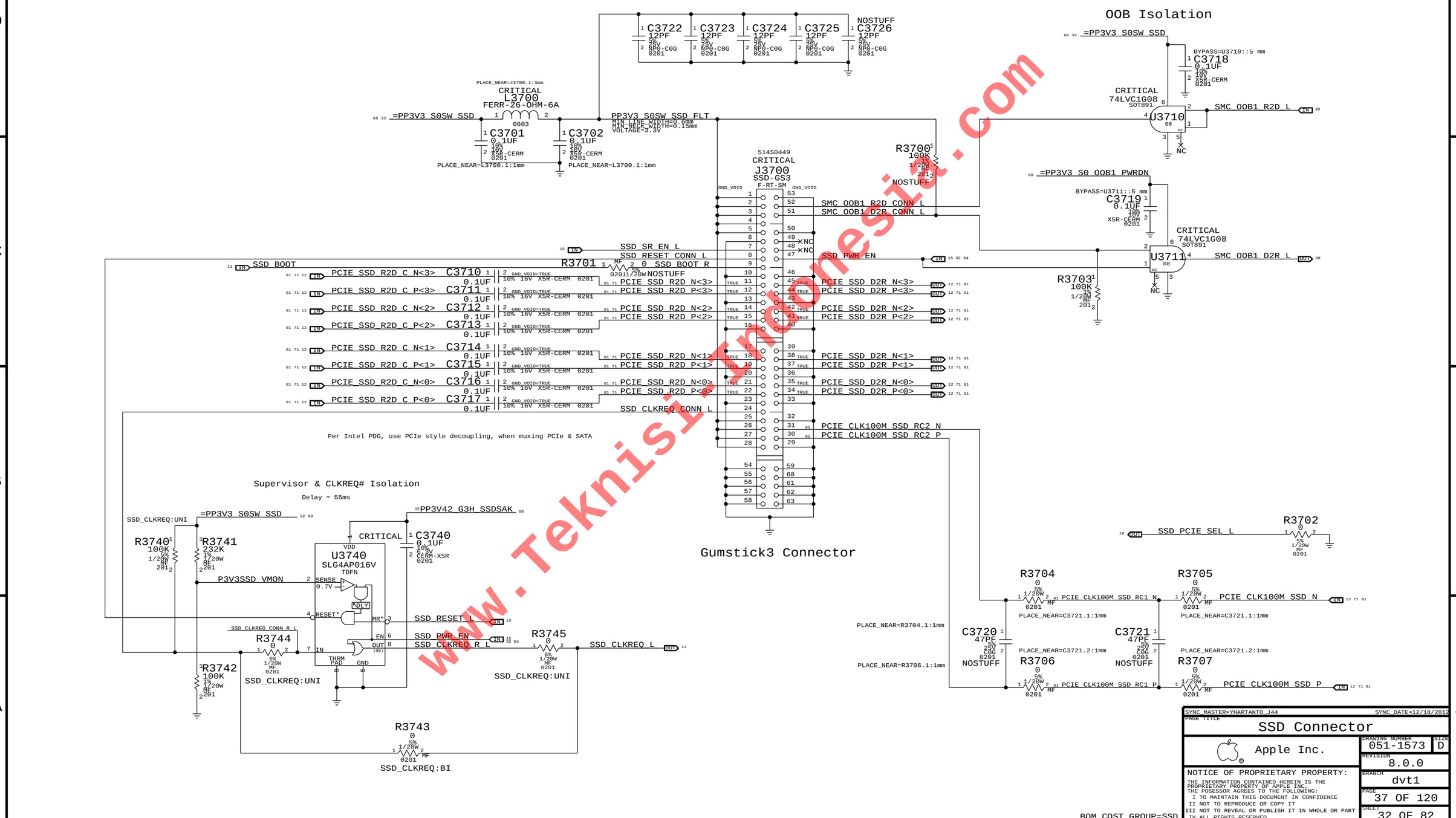

www.Teknisi-Indonesia.com

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=12/18/2013

PAGE TITLE: SSD Connector

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 37 OF 120

SHEET: 32 OF 82

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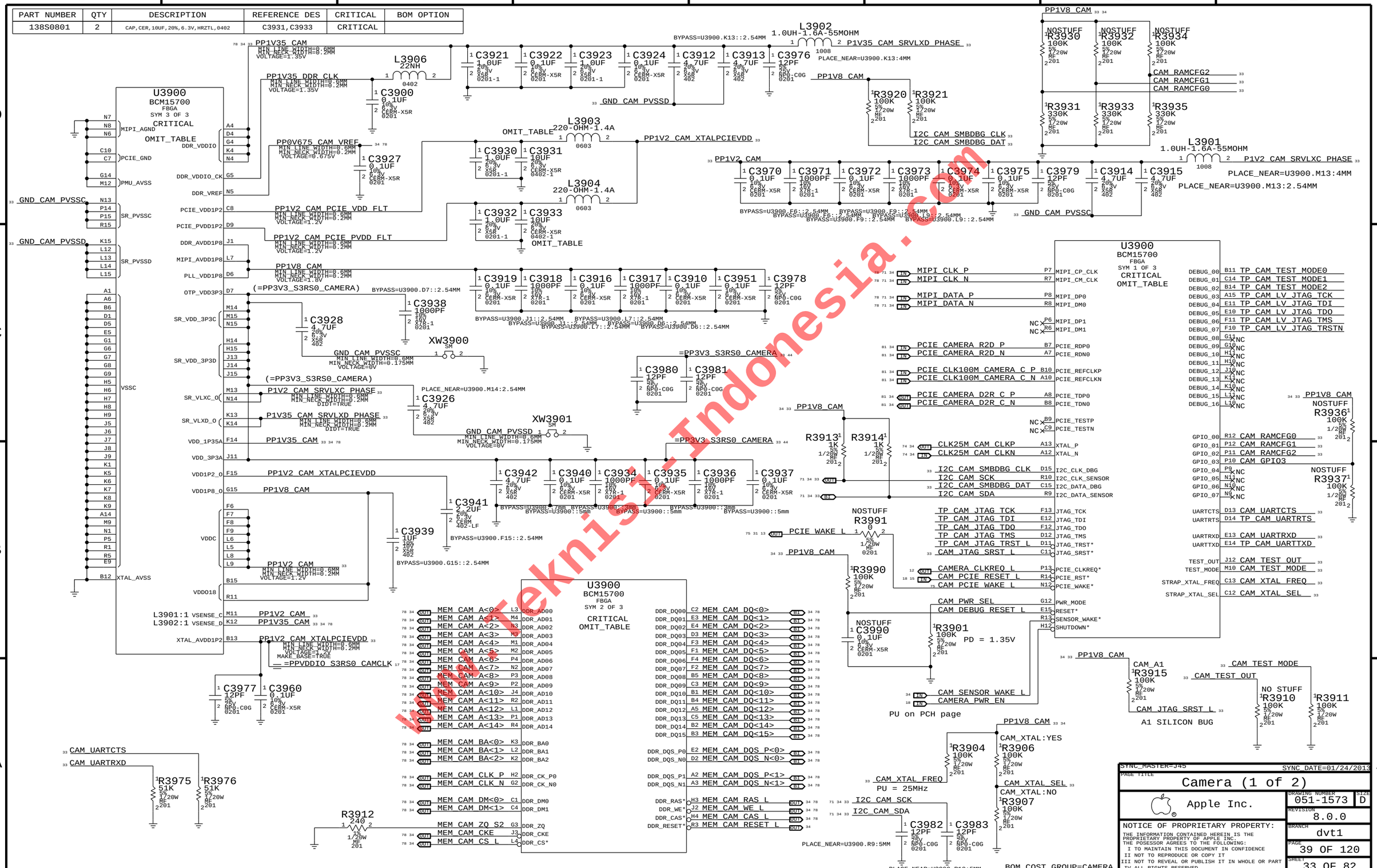
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	2	CAP,CER,10UF,20%,6.3V,HRZTL,0402	C3931,C3933	CRITICAL	



SYNC_MASTER=J45 SYNC_DATE=01/24/2013

PAGE TITLE: Camera (1 of 2)

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 39 OF 120

SHEET: 33 OF 82

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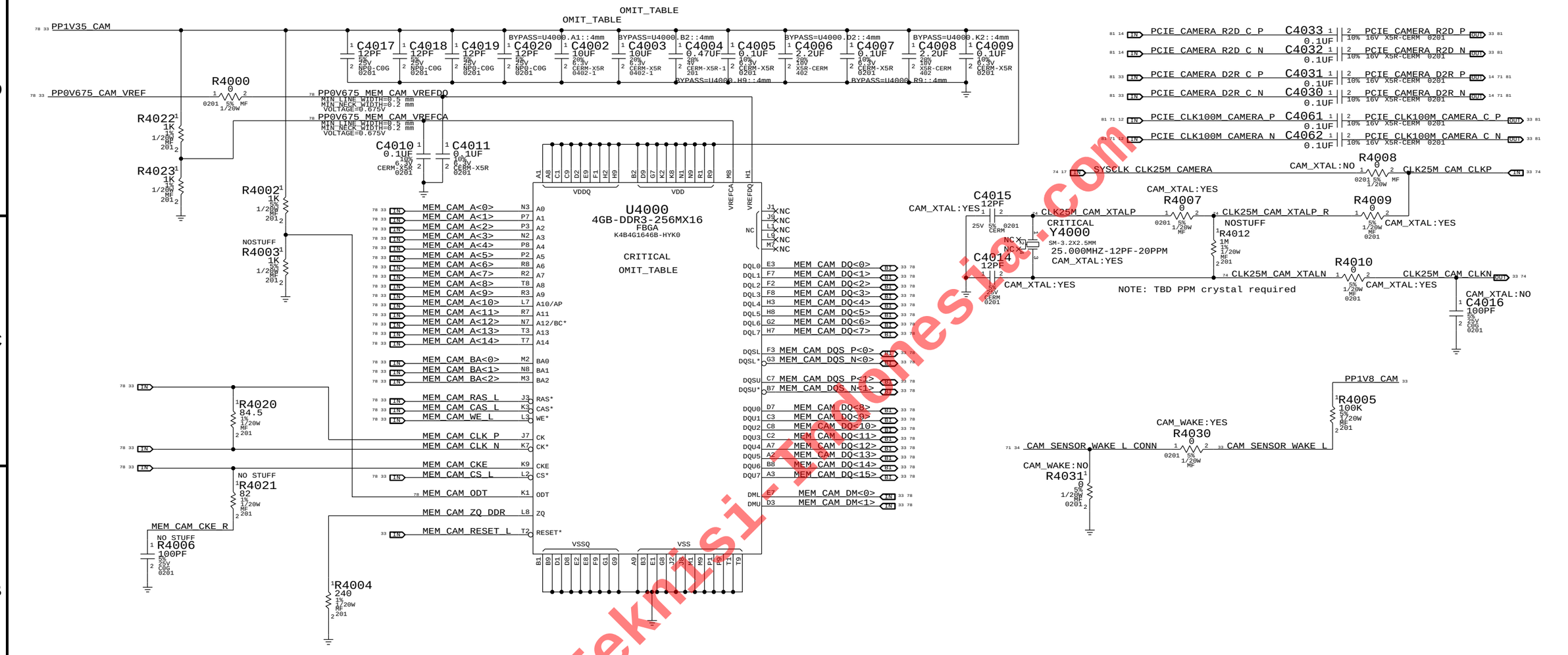
NotebookTechnician.com



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	2	CAP,CER,10UF,20%,6.3V,HRZTL,0402	C4002,C4003	CRITICAL	

BOM_COST_GROUP=CAMERA

SYNC_MASTER=J41 SYNC_DATE=12/21/2012

PAGE TITLE: Camera (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 40 OF 120

SHEET: 34 OF 82

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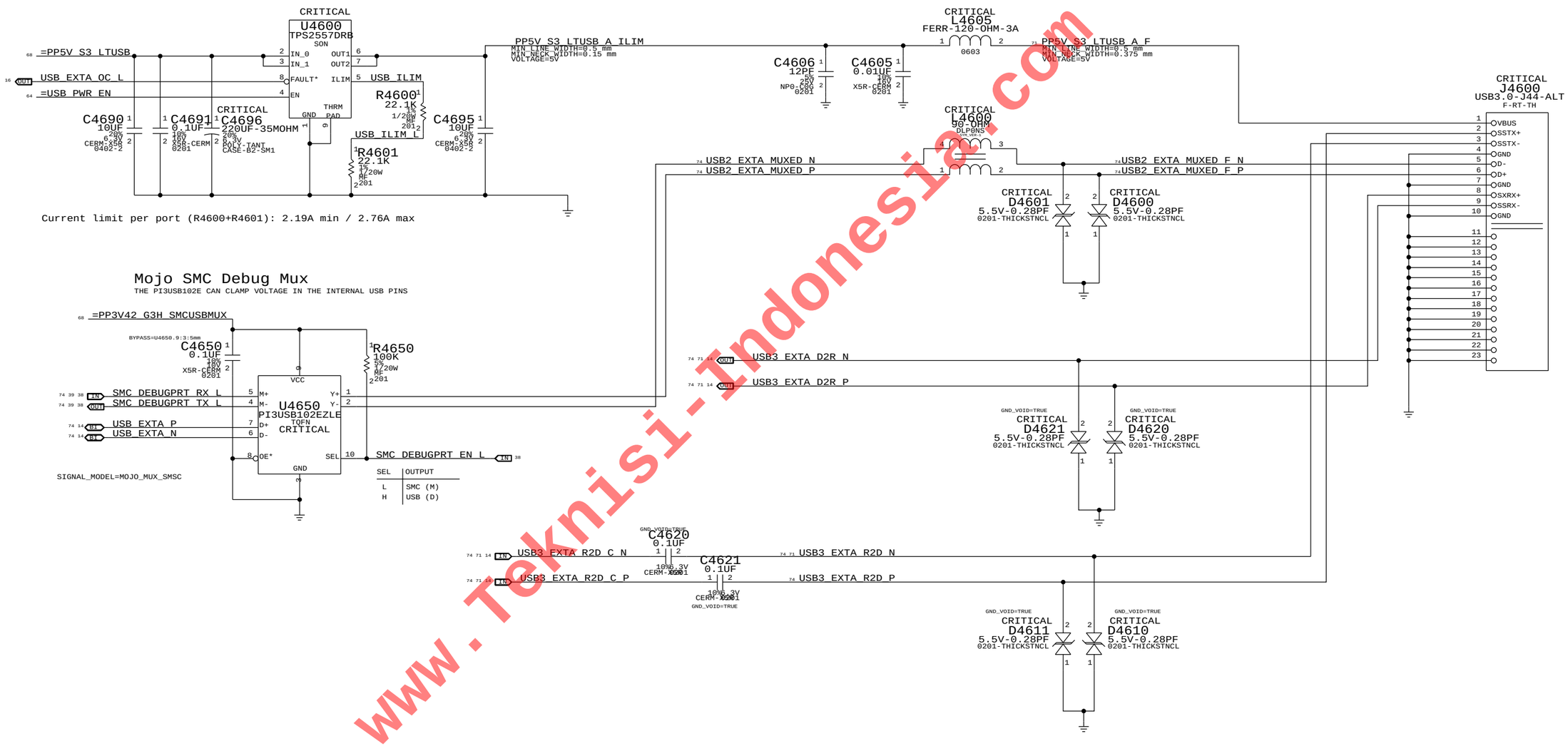
RIGHT USB PORT A

USB Port Power Switch



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BOM_COST_GROUP=IO PORTS

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE
External A USB3 Connector

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 46 OF 120

SHEET 35 OF 82

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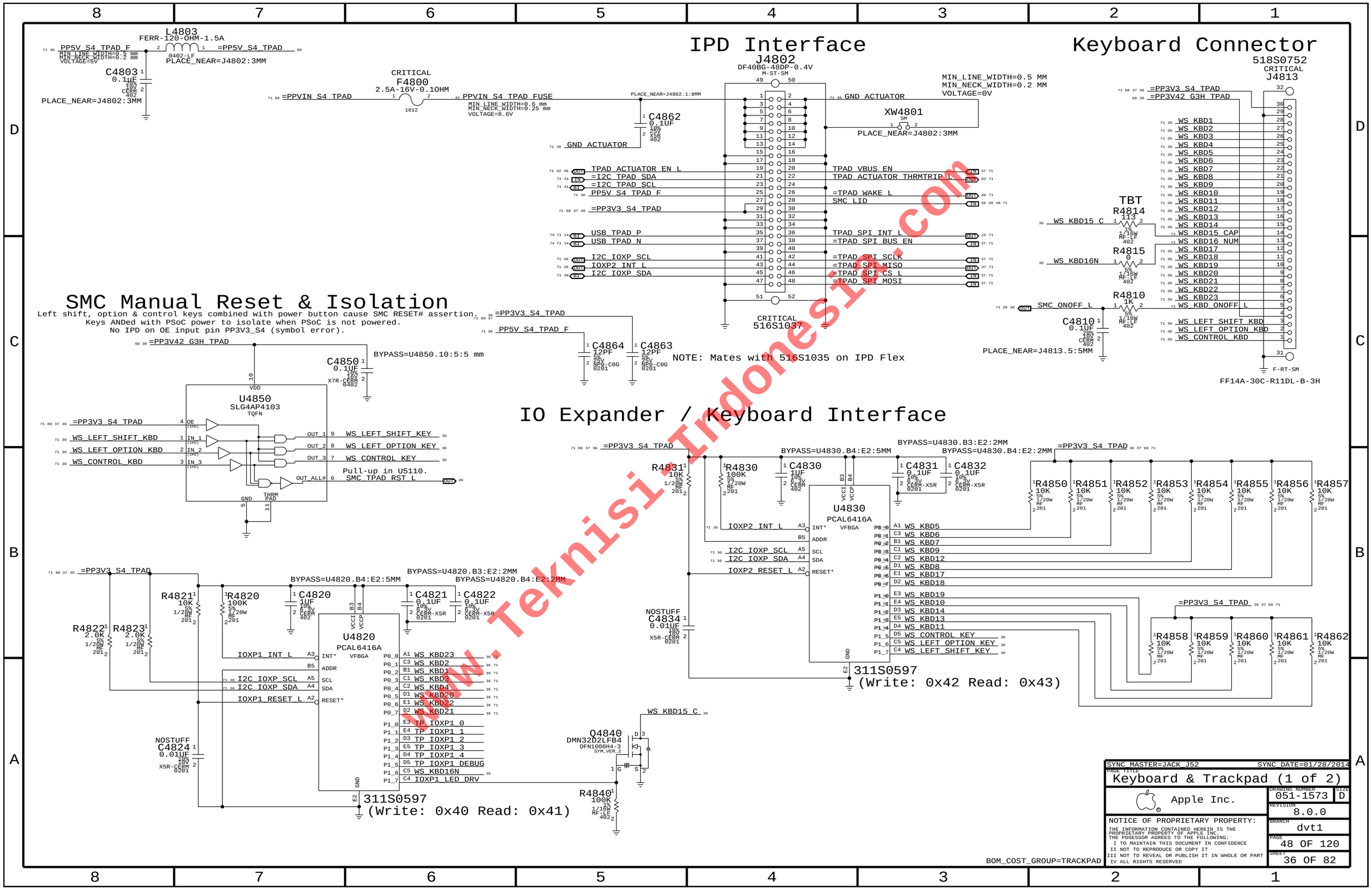

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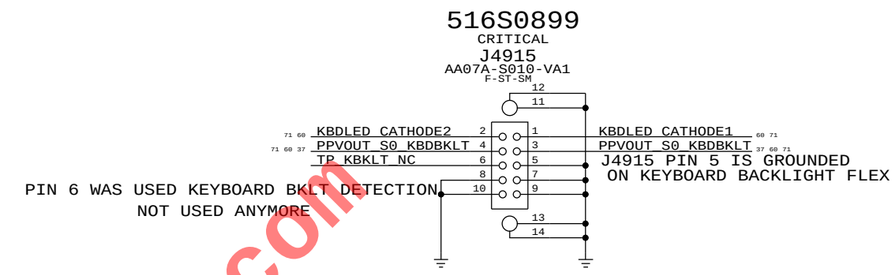
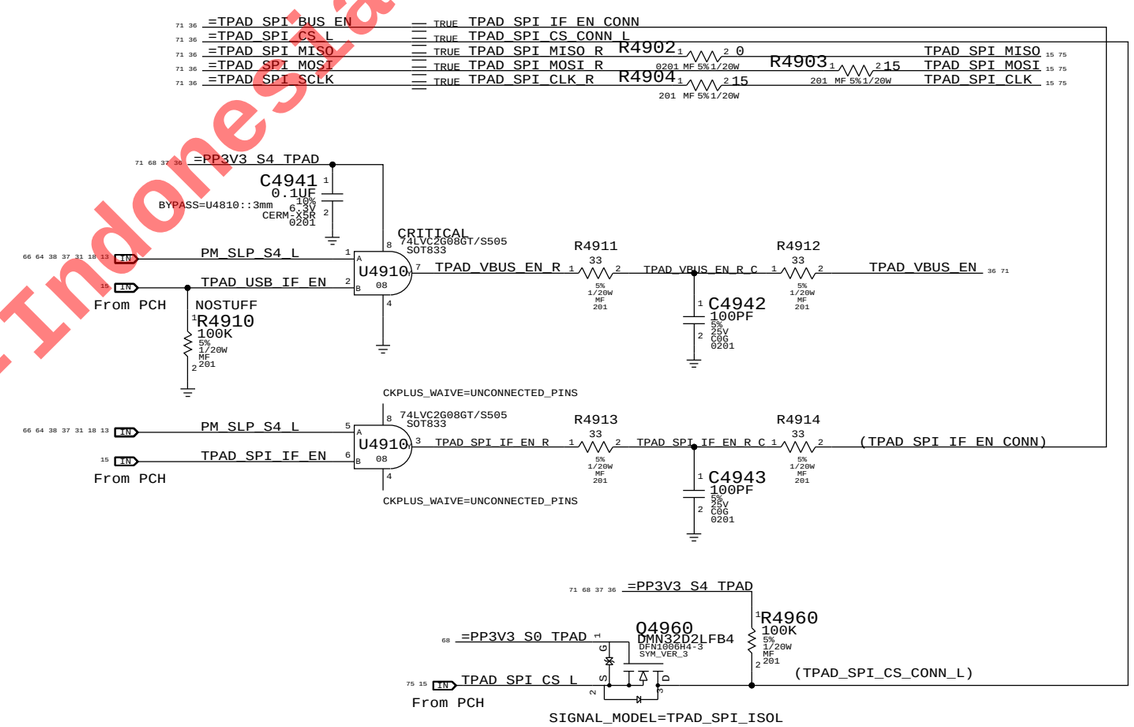
Keyboard Backlight Connector



TPAD SPI WITH SRC TERMINATION



BOM_COST_GROUP=TRACKPAD

SYNC MASTER=JACK J58 SYNC DATE=01/31/2014

PAGE TITLE
Keyboard & Trackpad (2 of 2)

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 49 OF 120

SHEET 37 OF 82

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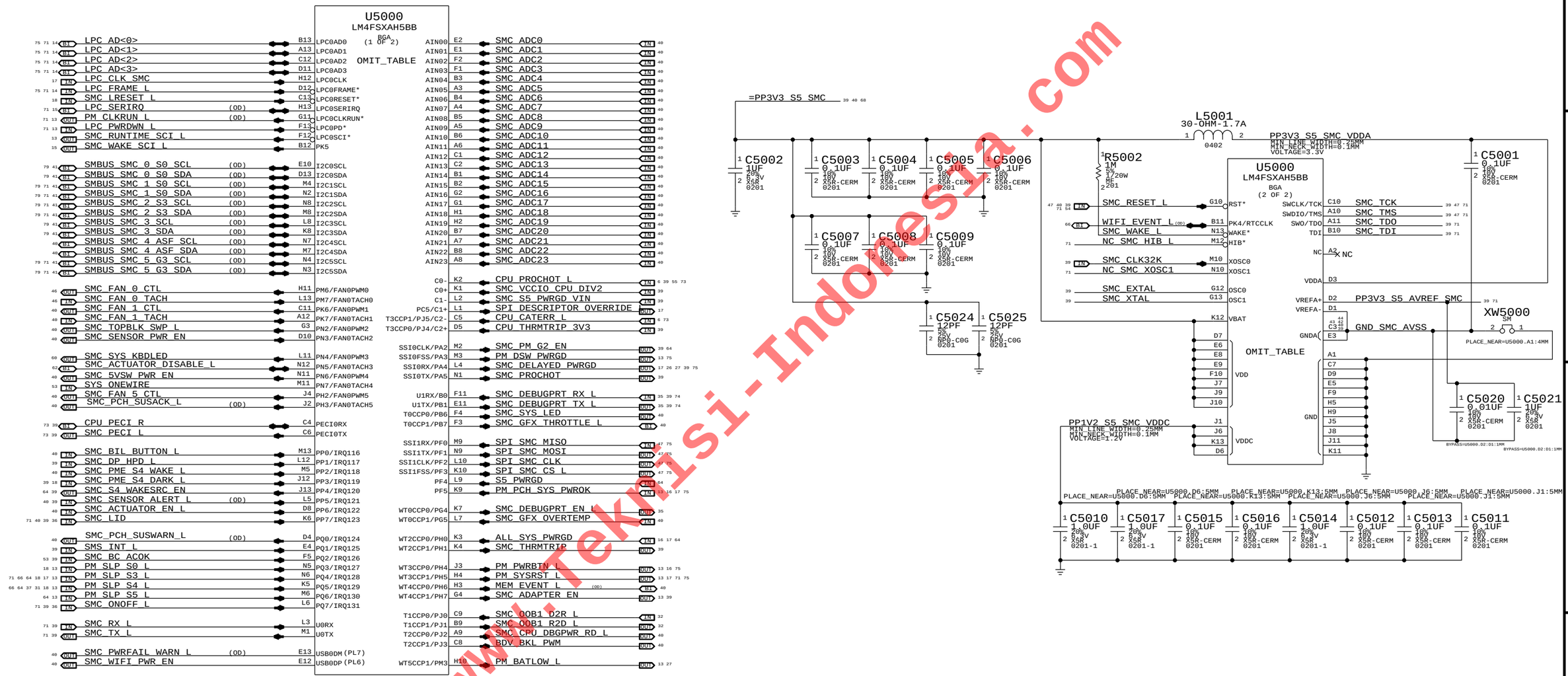

NOTE:
SMS INTERRUPT IS NOT USED, PULL UP TO SMC RAIL.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

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BOM_COST_GROUP=SMC

SYNC_MASTER=JACK_J52 SYNC_DATE=11/07/2013

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 50 OF 120

SHEET: 38 OF 82

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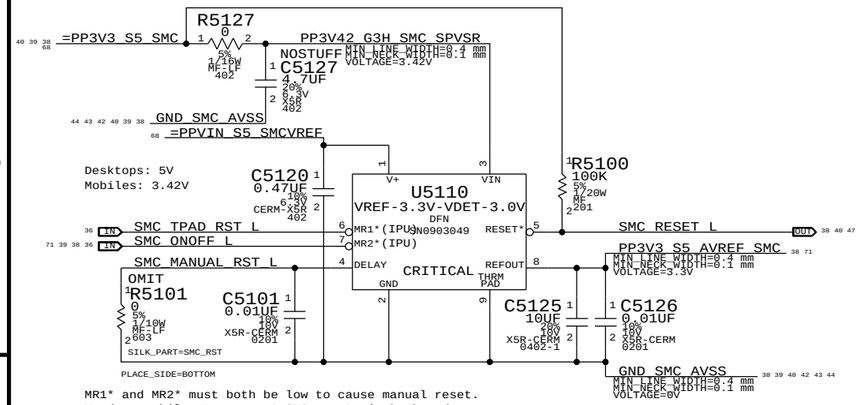
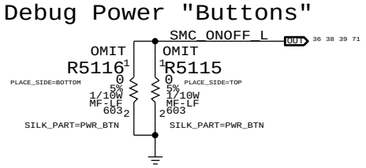
SMC Reset "Button", Supervisor & AVREF Supply



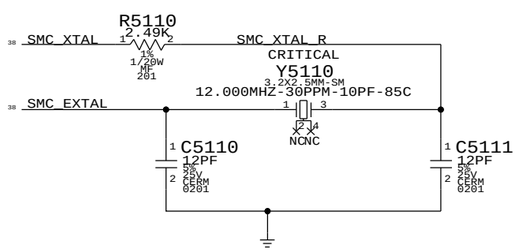
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

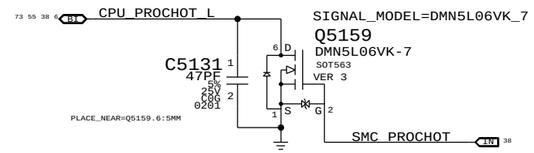
Debug Power "Buttons"

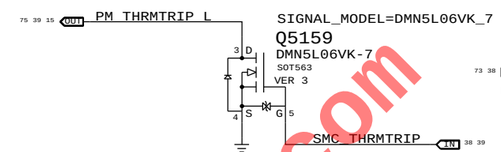


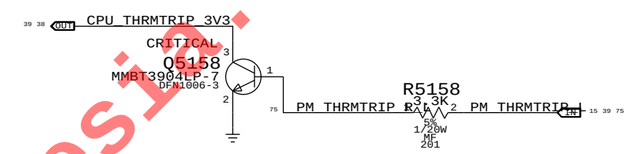
SMC Crystal Circuit

SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz

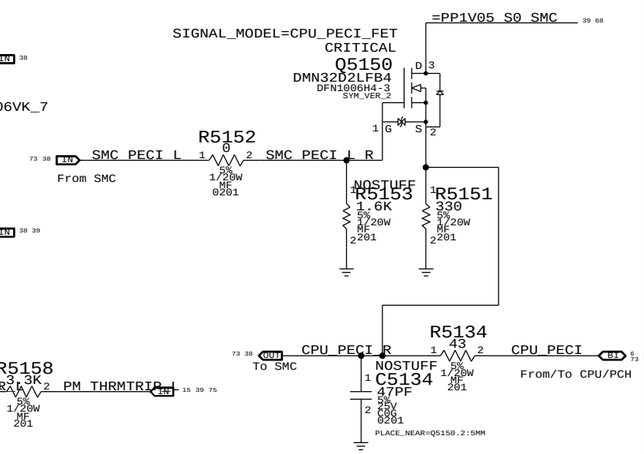


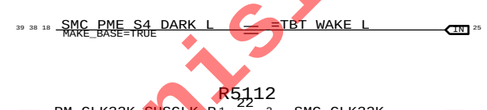


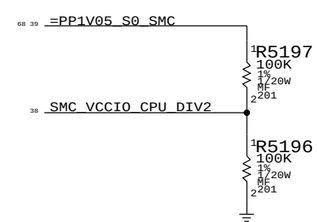


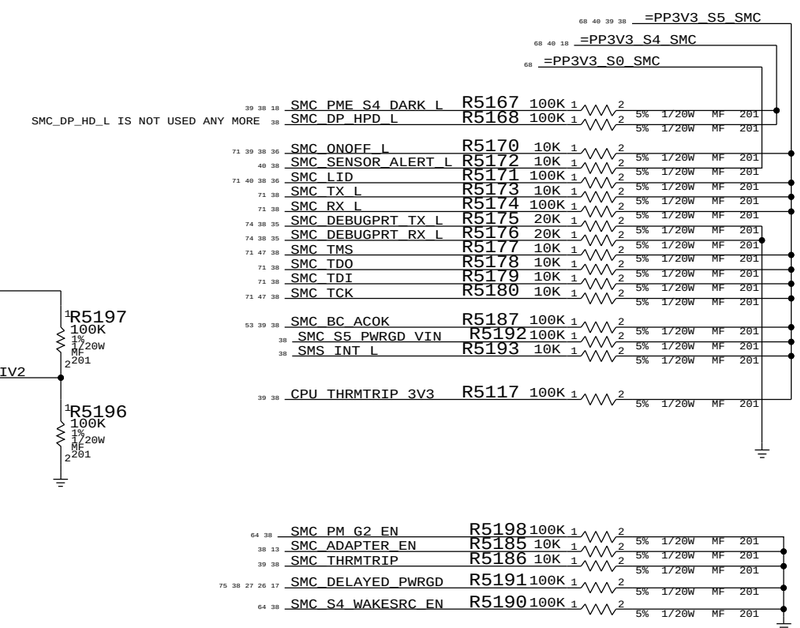


SMC12 PECI Support









BOM_COST_GROUP=SMC

SYNC_MASTER=JACK_J52 SYNC_DATE=10/24/2013

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 51 OF 120

SHEET: 39 OF 82

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SMC12 ADC Assignments

SMC_ADC0	SMC_CPU_HI_ISENSE (MAKE_BASE=TRUE)
SMC_ADC1	SMC_PBUS_VSENSE (MAKE_BASE=TRUE)
SMC_ADC2	SMC_BMON_ISENSE (MAKE_BASE=TRUE)
SMC_ADC3	SMC_DCIN_ISENSE (MAKE_BASE=TRUE)
SMC_ADC4	SMC_DCIN_VSENSE (MAKE_BASE=TRUE)
SMC_ADC5	SMC_BMON_DISCRETE_ISENSE (MAKE_BASE=TRUE)
SMC_ADC6	SMC_CPU_ISENSE (MAKE_BASE=TRUE)
SMC_ADC7	SMC_OTHER5V_HI_ISENSE (MAKE_BASE=TRUE)
SMC_ADC8	SMC_OTHER3V3_HI_ISENSE (MAKE_BASE=TRUE)
SMC_ADC9	SMC_DDR_ISENSE (MAKE_BASE=TRUE)
SMC_ADC10	SMC_LCDBKLT_ISENSE (MAKE_BASE=TRUE)
SMC_ADC11	SMC_TPAD_ISENSE (MAKE_BASE=TRUE)
SMC_ADC12	SMC_DDR1V8_ISENSE (MAKE_BASE=TRUE)
SMC_ADC13	SMC_SSD_ISENSE (MAKE_BASE=TRUE)
SMC_ADC14	SMC_PP3V3S0_ISENSE (MAKE_BASE=TRUE)
SMC_ADC15	SMC_CAMERA_ISENSE (MAKE_BASE=TRUE)
SMC_ADC16	SMC_TPAD_VSENSE (MAKE_BASE=TRUE)
SMC_ADC17	SMC_PP5VS0_ISENSE (MAKE_BASE=TRUE)
SMC_ADC18	SMC_CPUDDR_ISENSE (MAKE_BASE=TRUE)
SMC_ADC19	SMC_PCH_ISENSE (MAKE_BASE=TRUE)
SMC_ADC20	SMC_CPU_VSENSE (MAKE_BASE=TRUE)
SMC_ADC21	SMC_LCDPANEL_ISENSE (MAKE_BASE=TRUE)
SMC_ADC22	SMC_CPU_IMON_ISENSE (MAKE_BASE=TRUE)
SMC_ADC23	SMC_TBT_ISENSE (MAKE_BASE=TRUE)

SMC12 Pin Assignments

SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA (MAKE_BASE=TRUE, NO_TEST=TRUE)
BDV_BKL_PWM	NC_SMC_TPAD_BOOST_DISABLE_L (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_SYS_LED	NC_SMC_SYS_LED (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_5VSW_PWR_EN	NC_SMC_5VSW_PWR_EN (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_FAN_5_CTL	NC_SMC_FAN_5_CTL (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_BIL_BUTTON_L	NC_SMC_BIL_BUTTON_L (MAKE_BASE=TRUE, NO_TEST=TRUE)
MEM_EVENT_L	NC_MEM_EVENT_L (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_PWRFAIL_WARN_L	NC_SMC_PWRFAIL_WARN_L (MAKE_BASE=TRUE, NO_TEST=TRUE)

Thermal Alerts

PCH_SML1ALERT_L	NOSTUFF R5215 100 5% 1/20W MF 201		
SMC_CPUHI_COMP_ALERT_L	CPUHYS R5217 100 5% 1/20W MF 201		
SMC_BMON_COMP_ALERT_L	BMONHYS R5213 100 5% 1/20W MF 201		
CPUTHMSNS_THM_L	R5216 100 5% 1/20W MF 201	CPUTHRM_THRM:SMC	
CPUTHMSNS_ALERT_L	R5214 100 5% 1/20W MF 201	CPUTHRM_ALRT:SMC	
TBTTHMSNS_THM_L	R5220 100 5% 1/20W MF 201	TBTTHRM_THRM:SMC	
TBTTHMSNS_ALERT_L	R5210 100 5% 1/20W MF 201	TBTTHRM_ALRT:SMC	

SMC_SENSOR_ALERT_L (OUT)

=PP3V3_S5_SMC

R5232 10K 5% 1/20W MF 201 — SMCBOARDID:16

SMC_CPU_DBGPWR_RD_L — SMC_BOARDID (MAKE_BASE=TRUE)

R5233 10K 5% 1/20W MF 201 — SMCBOARDID:8

Hall Effect Pads

APN: 998-00296

OMIT_TABLE

J5250 HALL-EFFECT-MLB-J44 SM

=PP3V42_G3H_HALL

NC, NC, NC, NC

SMC_LID_R — R5250 0 5% 1/10W MF 402 — SMC_LID

C5250 0.001UF 10% 50V X7R-CERM 0402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-01216	1	SUBASSY,PCBA,HALL EFFECT,X304	J5250	CRITICAL	

639-00525 (PCBA,HALL EFFECT,X304) REPORTS TO 677-01216

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:PU
CPUTHRM:ALRT	CPUTHRM_THRM:PU,CPUTHRM_ALRT:SMC
CPUTHRM:NONE	CPUTHRM_THRM:PU,CPUTHRM_ALRT:PU

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU

Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.

S4 SMC Wake Sources

=PP3V3_S4_SMC

R5282 100K 5% 1/20W MF 201

=TPAD_WAKE_L

BT_WAKE_L

SMC_PME_S4_WAKE_L (MAKE_BASE=TRUE) (OUT)

SMC_PCH_SUSWARN_L (MAKE_BASE=TRUE)	R5230 0 5% 1/20W MF 0201	PCH_SUSWARN_L (OUT)
SMC_PCH_SUSACK_L (MAKE_BASE=TRUE)	R5231 0 5% 1/20W MF 0201	PCH_SUSACK_L (IN)
SMC_SENSOR_PWR_EN (MAKE_BASE=TRUE)		P3V3S4SW_SNS_EN; PBUSVSENSE_EN
SMC_WIFI_PWR_EN (MAKE_BASE=TRUE)		PM_WLAN_EN

=PP3V3_S4_SMC

SMC_WIFI_PWR_EN — R5295 10K 5% 1/20W MF 201 NOSTUFF

SMC_SENSOR_PWR_EN — R5294 10K 5% 1/20W MF 201 NOSTUFF

Top Block Swap

=PP3V3R1V8_S0_PCH_VCCSDIO

R5296 1K 5% 1/20W MF 201

SMC_TOPBLK_SWP_L — R5283 1K 5% 1/20W MF 201 — PCH_STRP_TOPBLK_SWP_L (OUT)

TPAD_ACTUATOR_EN_L — R5297 100 1% 1/20W MF 201 — TPAD_ACTUATOR_EN_RC_L (MAKE_BASE=TRUE) — SMC_ACTUATOR_EN_L

RC Placeholder to filter noise on this signal towards SMC IO.

C5271 220PF 10% 25V X7R-CERM 201

NOSTUFF C5270 1000PF 10% 16V X7R-1 0201

SMC_RESET_L

GND_SMC_AVSS

BOM_COST_GROUP=SMC

PAGE TITLE	SMC Project Support
	Apple Inc.
DRAWING NUMBER	051-1573
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WILDCAT POINT LP S0 "SMBus 0" Connections

68 41 =PP3V3_S0_SMBUS_PCH

WILDCAT POINT LP
U0500
(MASTER)
75 71 14 SMBUS_PCH_CLK MAKE_BASE=TRUE
75 71 14 SMBUS_PCH_DATA MAKE_BASE=TRUE

R5300 1K 5% 1/20W MF 201
R5301 1K 5% 1/20W MF 201

HDMI Redriver (on RIO)
J9510
(WRITE: 0xCC READ: 0xCD)
=I2C_HDMIRDRV_SCL 66
=I2C_HDMIRDRV_SDA 66

XDP Connectors
J1800
(MASTER)
16 =SMBUS_XDP_SCL
16 =SMBUS_XDP_SDA

WILDCAT POINT LP S0 "SMLink 0" Connections

68 41 =PP3V3_S0_SMBUS_PCH

WILDCAT POINT LP
U0500
(MASTER)
75 14 SML_PCH_0_CLK MAKE_BASE=TRUE
75 14 SML_PCH_0_DATA MAKE_BASE=TRUE

R5310 8.2K 5% 1/20W MF 201
R5311 8.2K 5% 1/20W MF 201

WILDCAT POINT LP S0 "SMLink 1" Connections

WILDCAT POINT LP
U0500
(Write: 0x88 Read: 0x89)
75 14 SML_PCH_1_CLK
75 14 SML_PCH_1_DATA

SMLink 1 is slave port to access PCH.

SMC SMBus "0" S0 Connections

65 15 PP3V3_S0_EDP_SW

SMC
U5000
(MASTER)
79 38 SMBUS_SMC_0_S0_SCL MAKE_BASE=TRUE
79 38 SMBUS_SMC_0_S0_SDA MAKE_BASE=TRUE

R5350 2.0K 5% 1/20W MF 201
R5351 2.0K 5% 1/20W MF 201

Internal DP
J8300
(See Table)
=I2C_TCON_SCL 65 71
=I2C_TCON_SDA 65 71

Internal DP

Parade T-con - (0x10-0x2F or 0x30-0x4F)

J44	Samsung	LGD
	Y	Y

SMC SMBus "2" S3 Connections

68 =PP3V3_S4_SMBUS_SMC_2

SMC
U5000
(MASTER)
79 71 38 SMBUS_SMC_2_S3_SCL MAKE_BASE=TRUE
79 71 38 SMBUS_SMC_2_S3_SDA MAKE_BASE=TRUE

R5370 1K 5% 1/20W MF 201
R5371 1K 5% 1/20W MF 201

Trackpad
J4802
(Write: 0x98 Read: 0x99)
=I2C_TPAD_SCL 36 71
=I2C_TPAD_SDA 36 71

SMC SMBus "1" S0 Connections

68 =PP3V3_S0_SMBUS_SMC_1

SMC
U5000
(MASTER)
79 71 38 SMBUS_SMC_1_S0_SCL MAKE_BASE=TRUE
79 71 38 SMBUS_SMC_1_S0_SDA MAKE_BASE=TRUE

R5360 2.0K 5% 1/20W MF 201
R5361 2.0K 5% 1/20W MF 201

CPU, Mem, Airflow, Fixstack Prox
EMC1704-02: U5870
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL 45
=I2C_CPUTHMSNS_SDA 45

ALS
J4002
(Write: 0x72 Read 0x73)
=I2C_ALS_SCL 34
=I2C_ALS_SDA 34

SMC SMBus "5" G3H Connections

68 =PP3V42_G3H_SMBUS_SMC_5

SMC
U5000
(MASTER)
79 71 38 SMBUS_SMC_5_G3_SCL MAKE_BASE=TRUE
79 71 38 SMBUS_SMC_5_G3_SDA MAKE_BASE=TRUE

R5380 2.0K 5% 1/20W MF 201
R5381 2.0K 5% 1/20W MF 201

Battery Charger
ISL6259 - U7100
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL 54
=SMBUS_CHGR_SDA 54

Battery
J7050
(See Table)
=SMBUS_BATT_SCL 53
=SMBUS_BATT_SDA 53

Battery

Battery Manager - (Write: 0x16 Read: 0x17)

SMC SMBus "3" S0 Connections

68 =PP3V3_S0_SMBUS_SMC_3

SMC
U5000
(MASTER)
79 38 SMBUS_SMC_3_SCL MAKE_BASE=TRUE
SMBUS_SMC_3_SDA MAKE_BASE=TRUE

R5390 2.0K 5% 1/20W MF 201
R5391 2.0K 5% 1/20W MF 201

X29 Temp (on RIO)
TMP105: J9510
(Write: 0x92 Read: 0x93)
=I2C_X29THMSNS_SCL 66
=I2C_X29THMSNS_SDA 66

TBT & MLB Prox
EMC1412: U5850
(Write: 0xD8 Read: 0xD9)
=I2C_TBTTHMSNS_SCL 45
=I2C_TBTTHMSNS_SDA 45

BOM_COST_GROUP=SMC

SYNC_MASTER=GKOO_J52 SYNC_DATE=12/06/2013

PAGE TITLE
SMBus Connections

Apple Inc.

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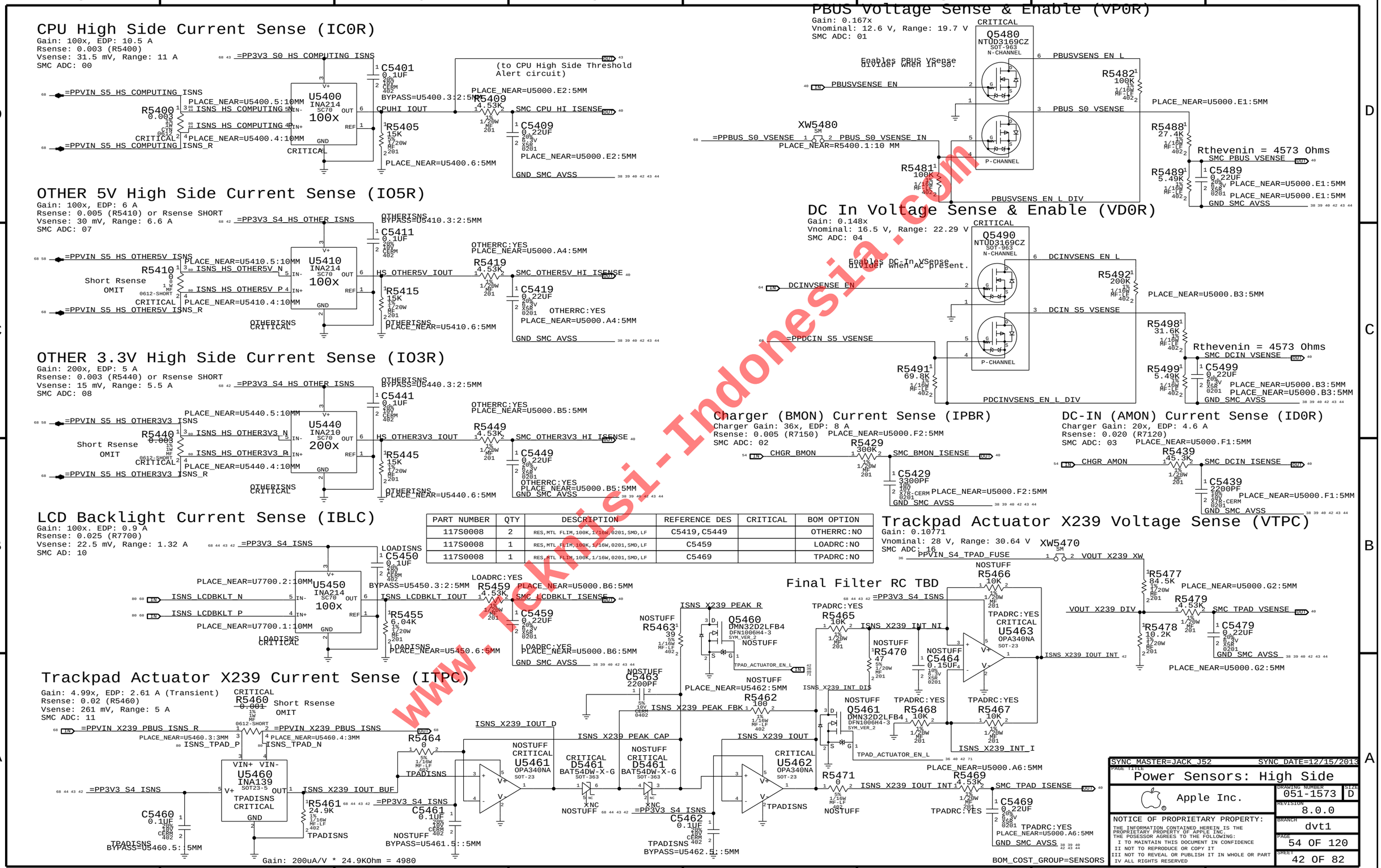

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		TPADRC:NO

SYNC MASTER=JACK_J52 SYNC DATE=12/15/2013

PAGE TITLE: Power Sensors: High Side

Apple Inc.

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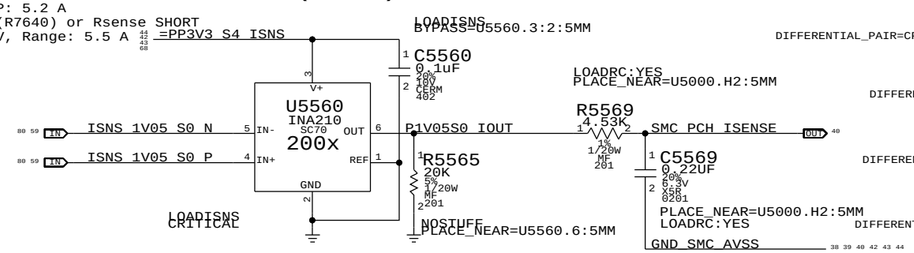
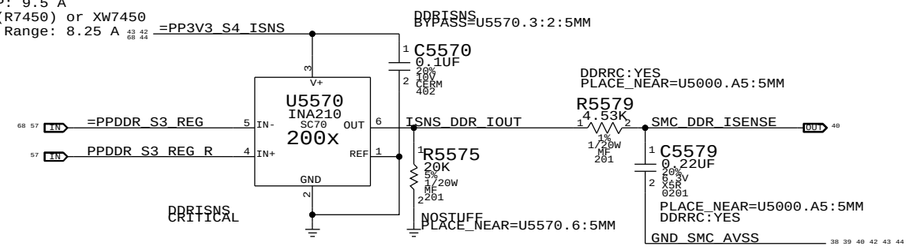
PCH 1.05V Current Sense (IC1C)

Gain: 200x, EDP: 5.2 A
Rsense: 0.003 (R7640) or Rsense SHORT
Vsense: 15.6 mV, Range: 5.5 A
SMC ADC: 19



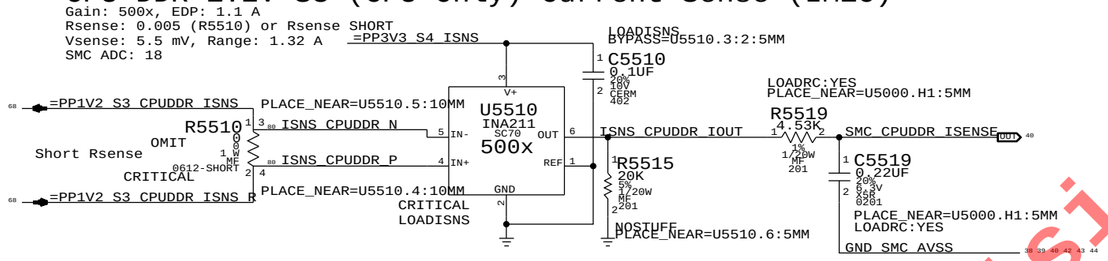
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 200x, EDP: 9.5 A
Rsense: 0.002 (R7450) or XW7450
Vsense: 19 mV, Range: 8.25 A
SMC ADC: 09



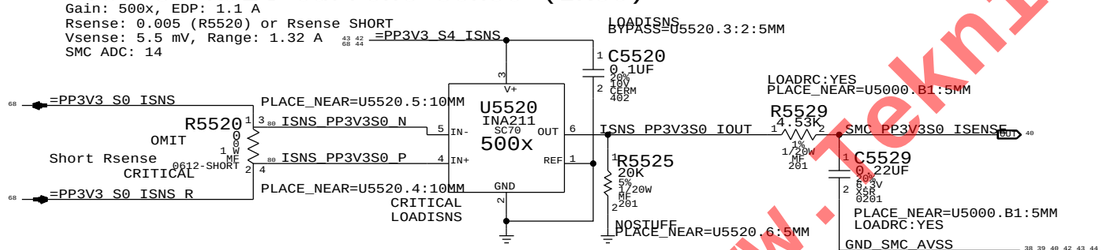
CPU DDR 1.2V S3 (CPU Only) Current Sense (IM1C)

Gain: 500x, EDP: 1.1 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 5.5 mV, Range: 1.32 A
SMC ADC: 18



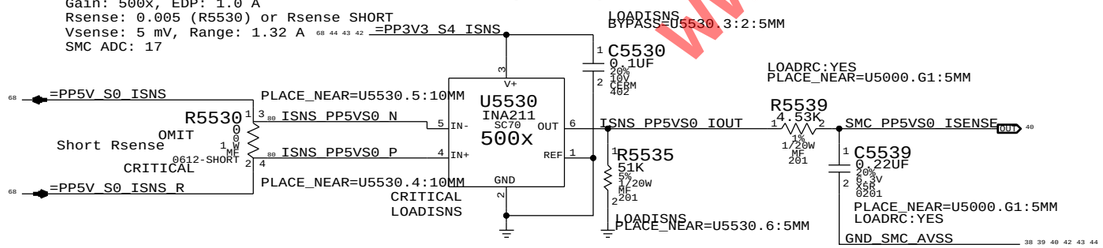
3.3V S0 Rail Current Sense (IR3C)

Gain: 500x, EDP: 1.1 A
Rsense: 0.005 (R5520) or Rsense SHORT
Vsense: 5.5 mV, Range: 1.32 A
SMC ADC: 14



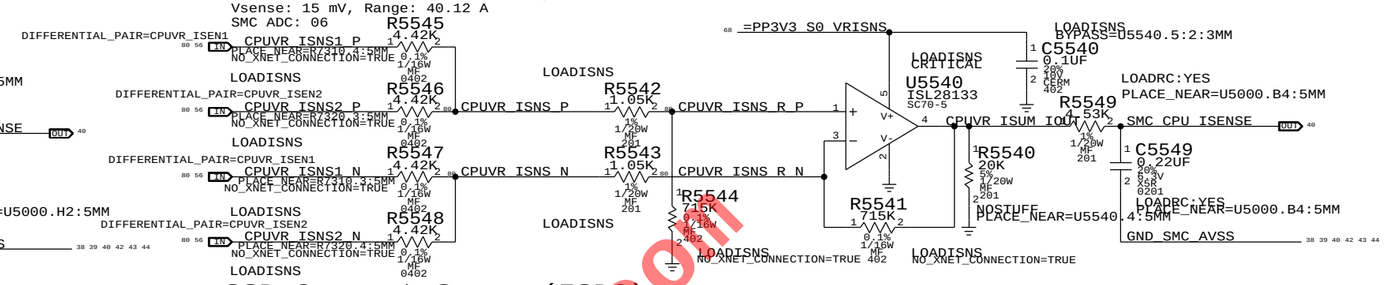
5V S0 Rail Current Sense (IR5C)

Gain: 500x, EDP: 1.0 A
Rsense: 0.005 (R5530) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC ADC: 17



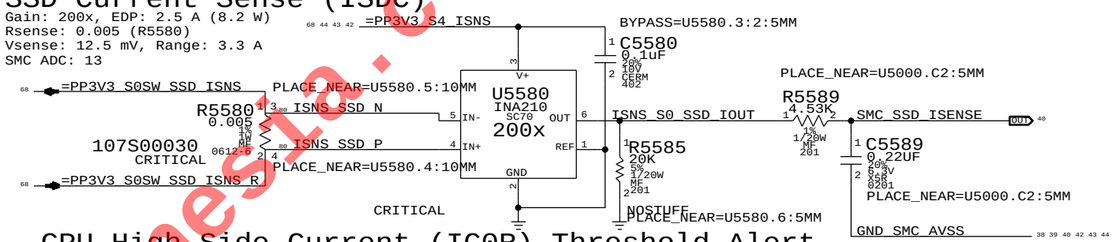
CPU Fixed Current Sense (IC0C)

Gain: 219.33x, EDP: 40 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 15 mV, Range: 40.12 A
SMC ADC: 06



SSD Current Sense (ISDC)

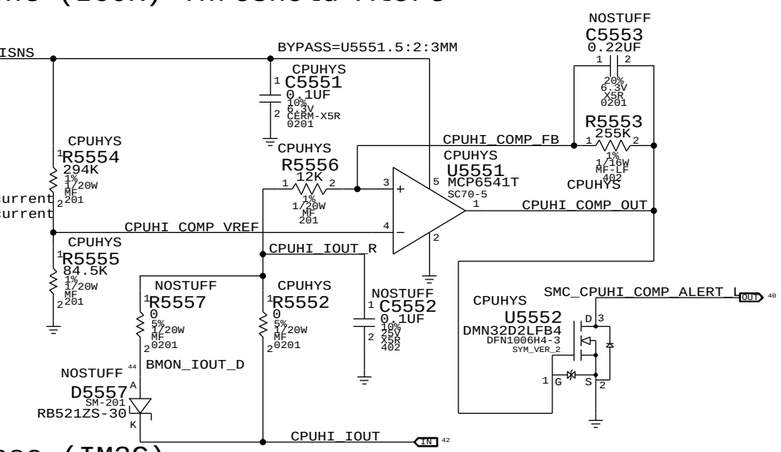
Gain: 200x, EDP: 2.5 A (8.2 W)
Rsense: 0.005 (R5580)
Vsense: 12.5 mV, Range: 3.3 A
SMC ADC: 13



CPU High Side Current (IC0R) Threshold Alert

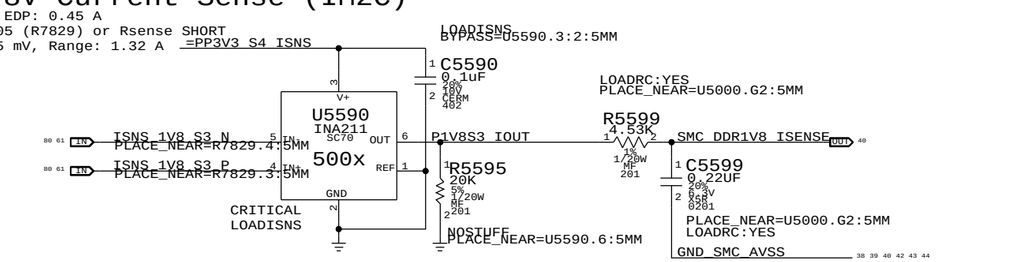
Gain: 100x
Rsense: 0.003 (R5400)

Trip Target on CPU High current: 2.5 A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vtl = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A



DDR 1.8V Current Sense (IM2C)

Gain: 500x, EDP: 0.45 A
Rsense: 0.005 (R7829) or Rsense SHORT
Vsense: 2.25 mV, Range: 1.32 A
SMC ADC: 12



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519,C5599		LOADRC:NO
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

BOM_COST_GROUP=SENSORS

SYNC_MASTER=JACK_J52 SYNC_DATE=12/06/2013

PAGE TITLE
Power Sensors: Load Side

Apple Inc.

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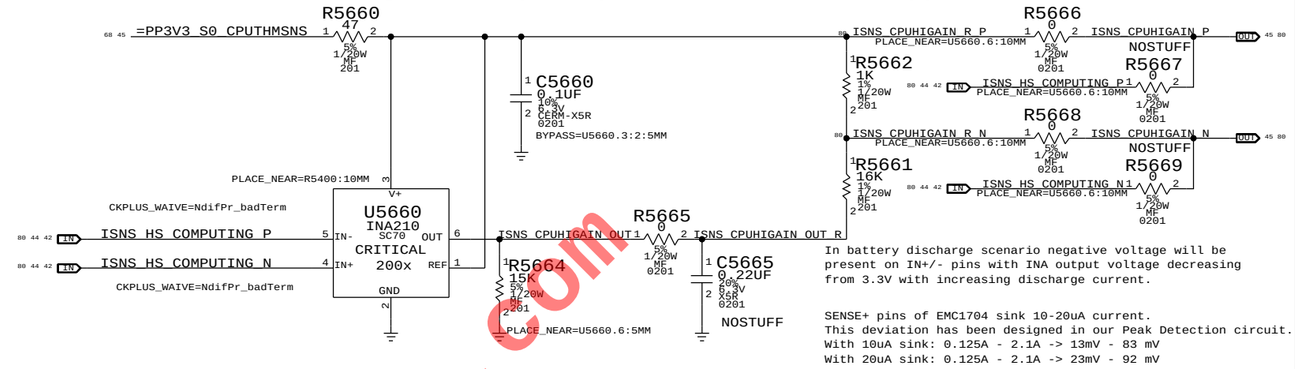
CPU High Side (IC0R) Peak Detection Support

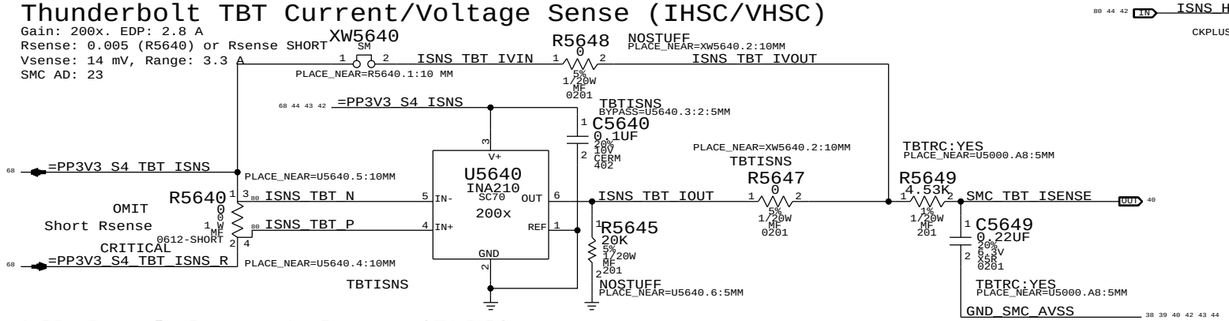


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit.
With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV
With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

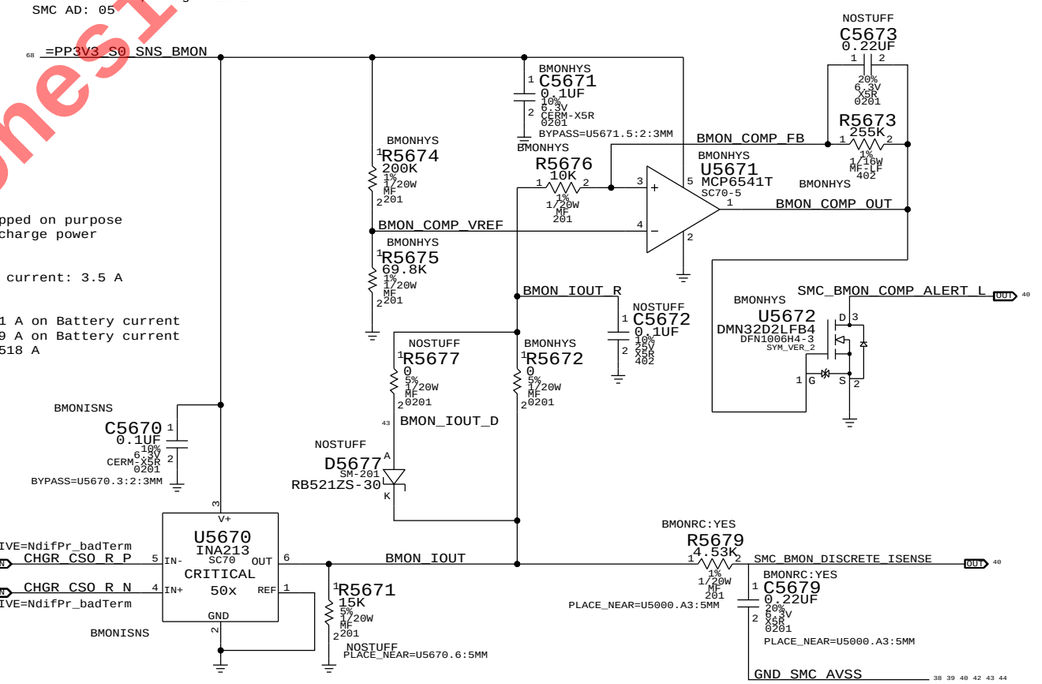
Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)

Gain: 200x. EDP: 2.8 A
Rsense: 0.005 (R5640) or Rsense SHORT
Vsense: 14 mV, Range: 3.3 A
SMC AD: 23



Battery BMON Discrete Current Sense (IP0R) & Threshold Alert

Gain: 50x. EDP: 8 A
Rsense: 0.005 (R7150)
Vsense: 50 mV, Range: 13.2 A
SMC AD: 05

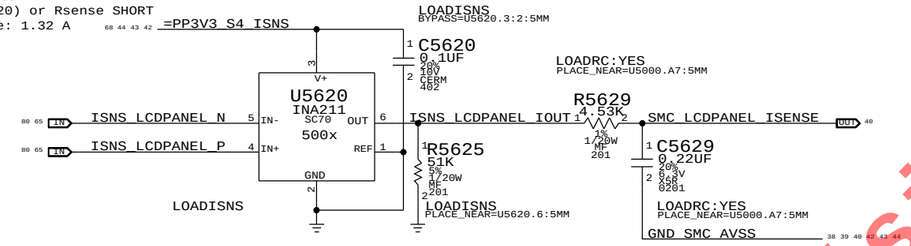


CHGR_CSO_R_P/N are swapped on purpose to measure battery discharge power into system.

Trip Target on Battery current: 3.5 A
Hysteresis Circuit:
Vref = 0.854 V
Vth = 0.758 V -> 3.031 A on Battery current
Vtl = 0.887 V -> 3.549 A on Battery current
Hysteresis Margin = 0.518 A

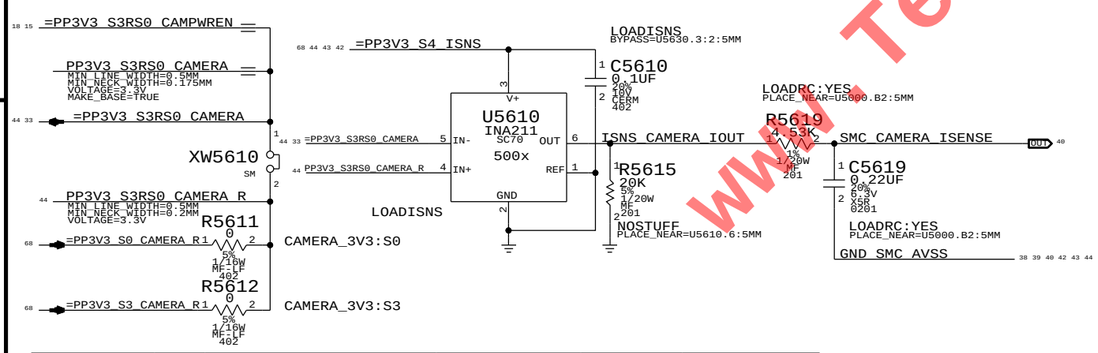
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
RSENSE: 0.005 (R8320) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC AD: 21



Camera (S2 Controller) Current Sense (ICMC)

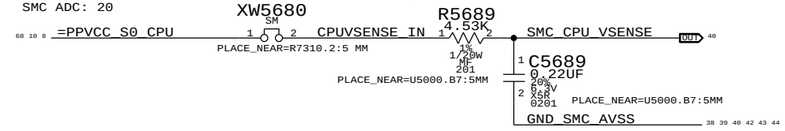
Gain: 500x. EDP: 0.82 A
Rsense: 0.005 (R5610) or XW5610
Vsense: 4.1 mV, Range: 1.32 A
SMC AD: 15



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629		LOADRC:NO
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5679		BMONRC:NO
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5649		TBTRC:NO

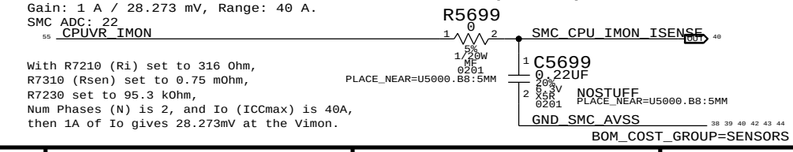
CPU Core Voltage Sense (VC0C)

SMC ADC: 20



CPU Core IMON Current Sense (IC2C)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 22



With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

BOM_COST_GROUP=SENSORS

SYNC_MASTER=JACK_J52 SYNC_DATE=10/26/2013

PAGE TITLE
Power Sensors: Extended

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
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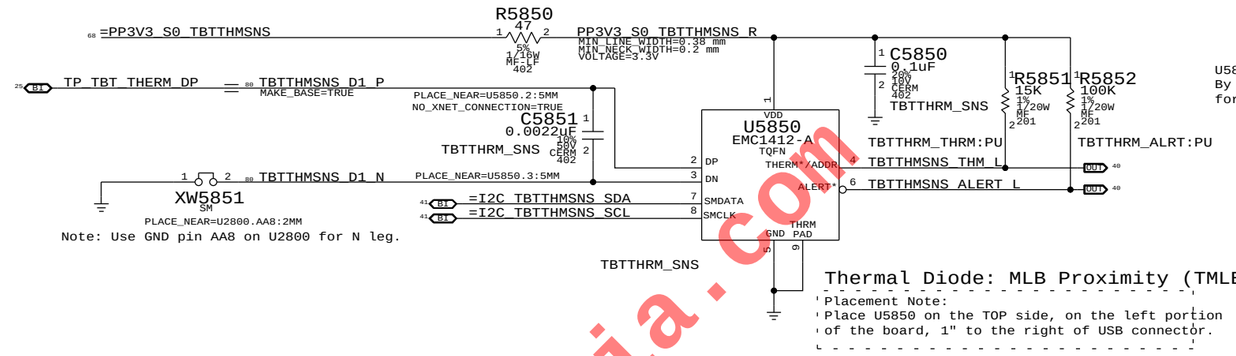
Thermal Sensor A:
Thunderbolt Die, MLB Proximity

I2C Write: 0xD8, I2C Read: 0xD9



U5850 I2C Address:
By setting R5851 to 15k, I2C address for U5850 is 0xD8/0xD9.

Thermal Diode: TBT Die (THSP)

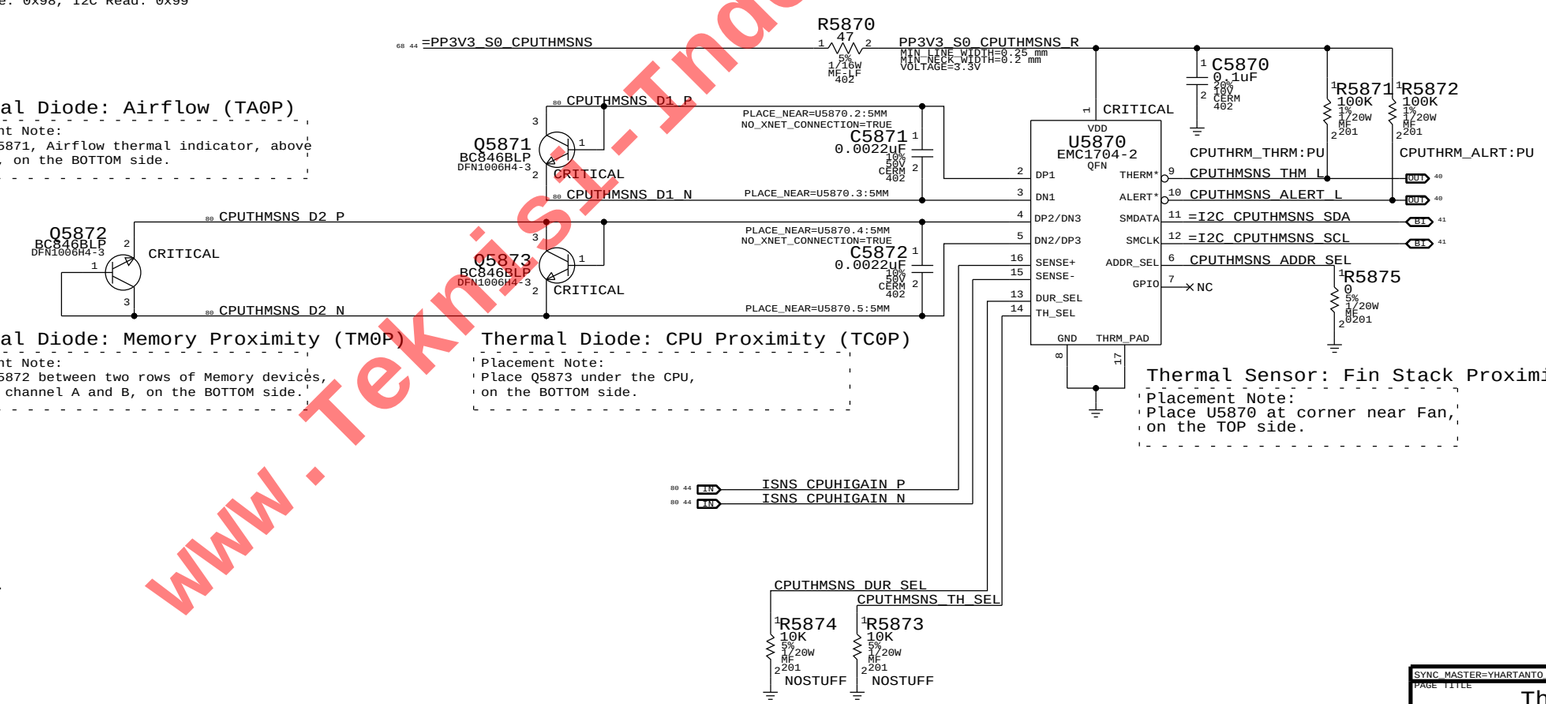
Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AA8.

Thermal Diode: MLB Proximity (TMLB)

Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Airflow (TA0P)

Placement Note:
Place Q5871, Airflow thermal indicator, above the SSD, on the BOTTOM side.

Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Diode: CPU Proximity (TC0P)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

Thermal Sensor: Fin Stack Proximity (Th1H)

Placement Note:
Place U5870 at corner near Fan, on the TOP side.

Placement Note: Place C5800 and C5801 near Q5871.

BOM_COST_GROUP=SENSORS

SYNC_MASTER=YHARTANTO_J44	SYNC_DATE=01/07/2013
PAGE TITLE: Thermal Sensors	
Apple Inc.	DRAWING NUMBER: 051-1573 / SIZE: D
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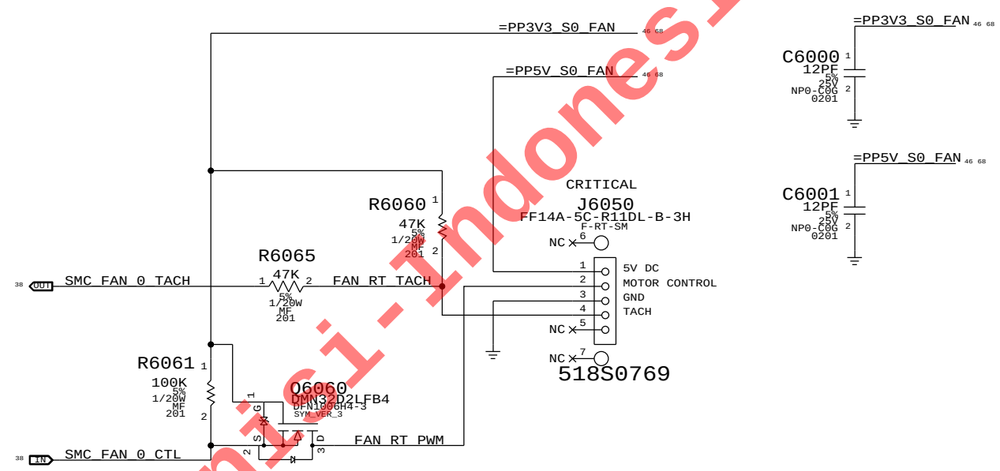
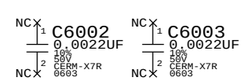
FAN CONNECTOR

KEEP THE 5 PIN CONNECTOR FROM D1



Placement Note: Place C6002 and C6003 near Q6060



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SYNC_MASTER=J41	SYNC_DATE=10/23/2012
PAGE TITLE	Fan
Apple Inc.	DRAWING NUMBER 051-1573 SIZE D
	REVISION 8.0.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH dvt1
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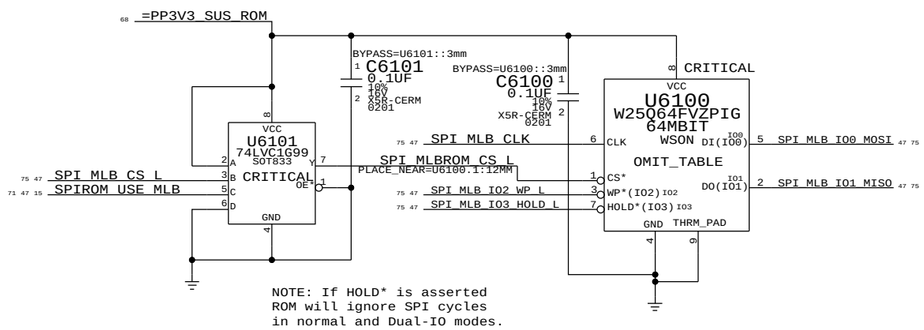
	SHEET 46 OF 82

BOM_COST_GROUP=FAN

SPI ROM

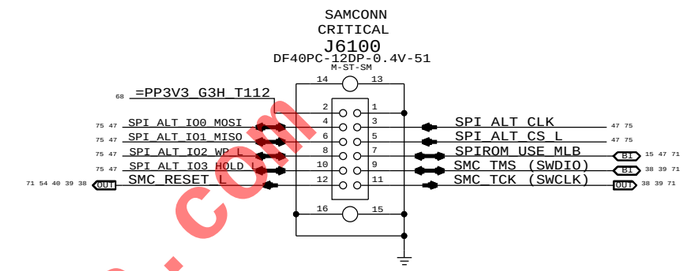
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



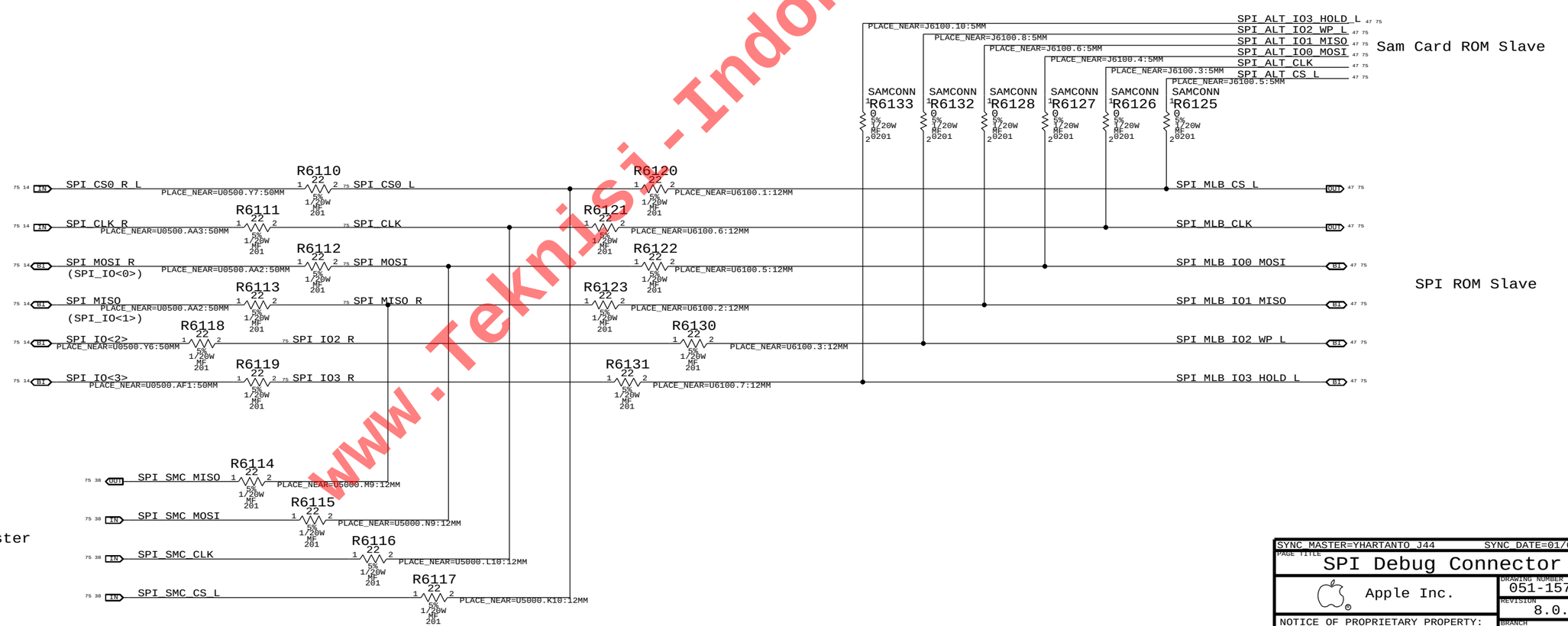
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination



BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 61 OF 120

SHEET: 47 OF 82

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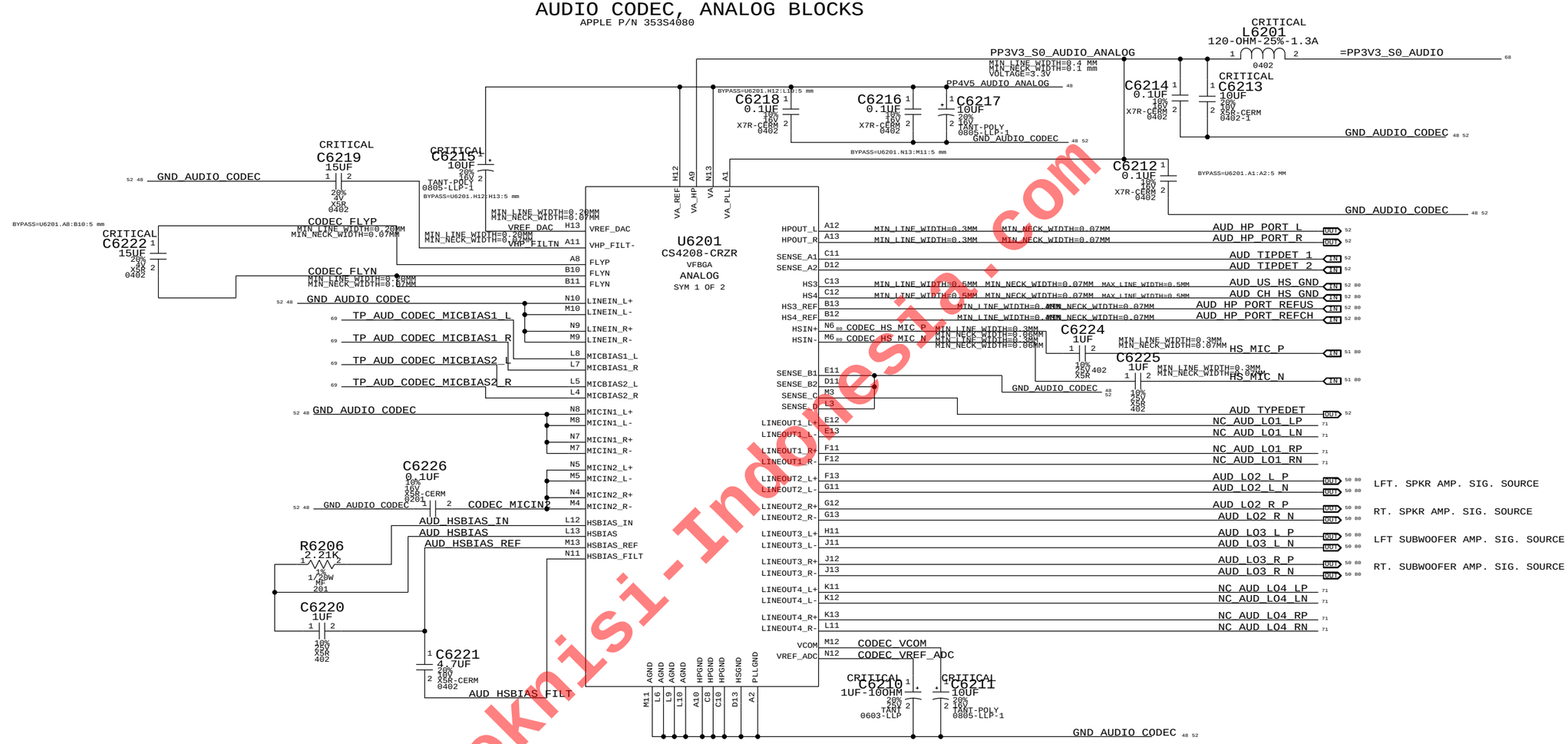
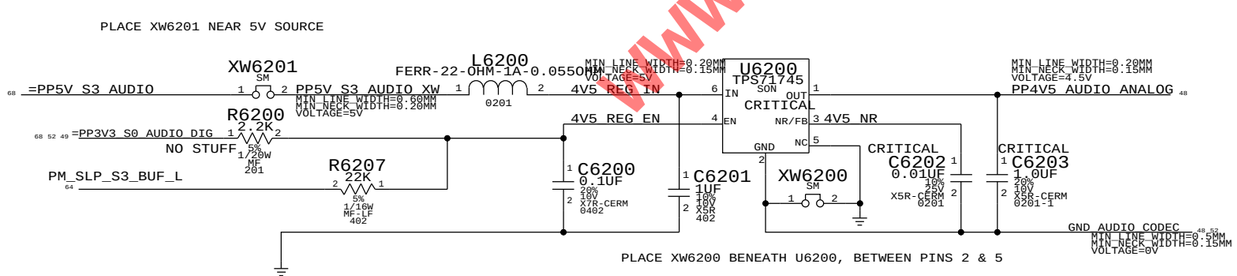
AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



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SYNC MASTER=JCURCIO_J44	SYNC DATE=05/13/2013
PAGE TITLE	Audio: Codec,Analog
Apple Inc.	DRAWING NUMBER 051-1573 · SIZE D
	REVISION 8.0.0
	BRANCH dvt1
	PAGE 62 OF 120
	SHEET 48 OF 82

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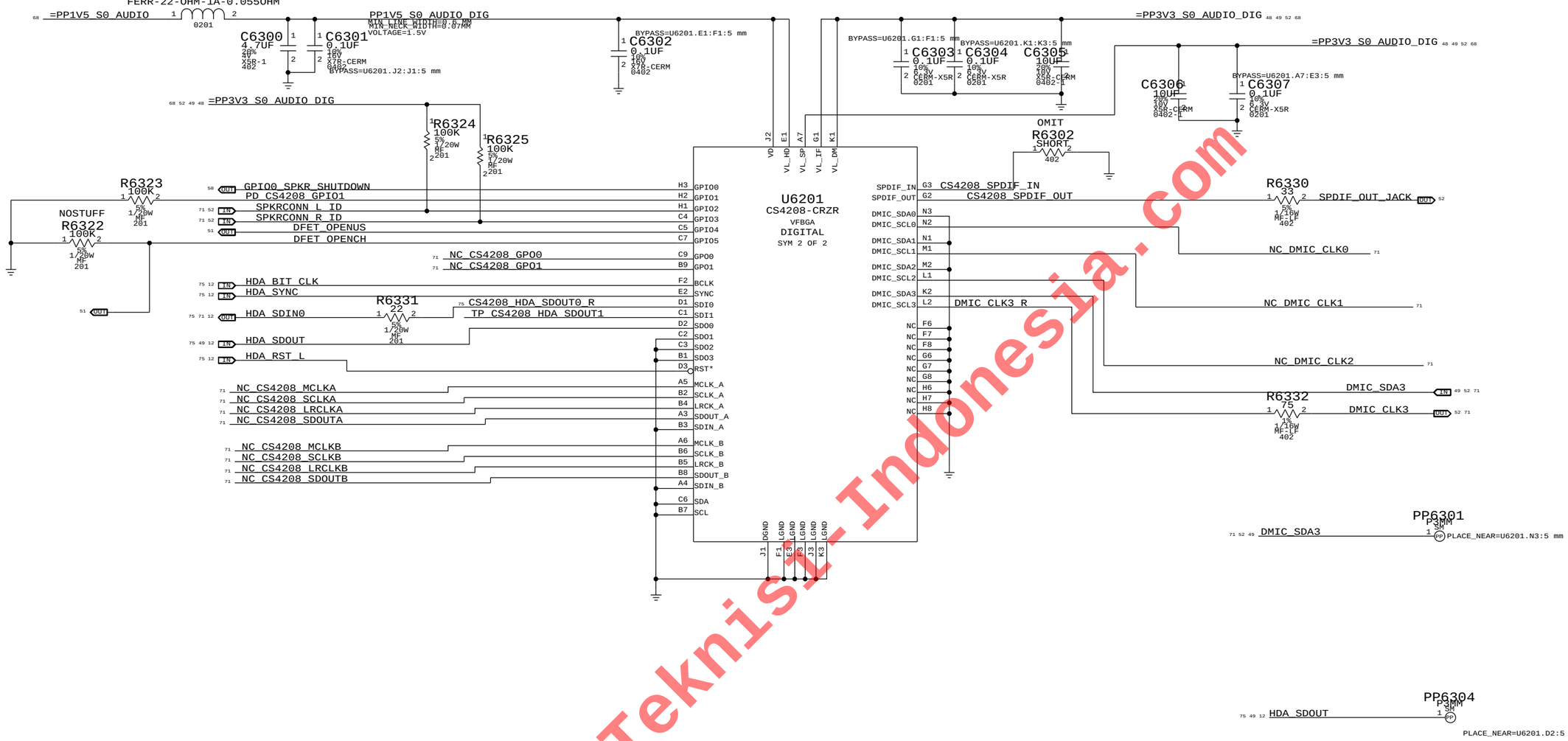
BOM_COST_GROUP=AUDIO

AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



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BOM_COST_GROUP=AUDIO

SYNC_MASTER=JCURCIO_J44 SYNC_DATE=07/25/2013

PAGE TITLE: Audio: Codec,Digital

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 63 OF 120

SHEET: 49 OF 82

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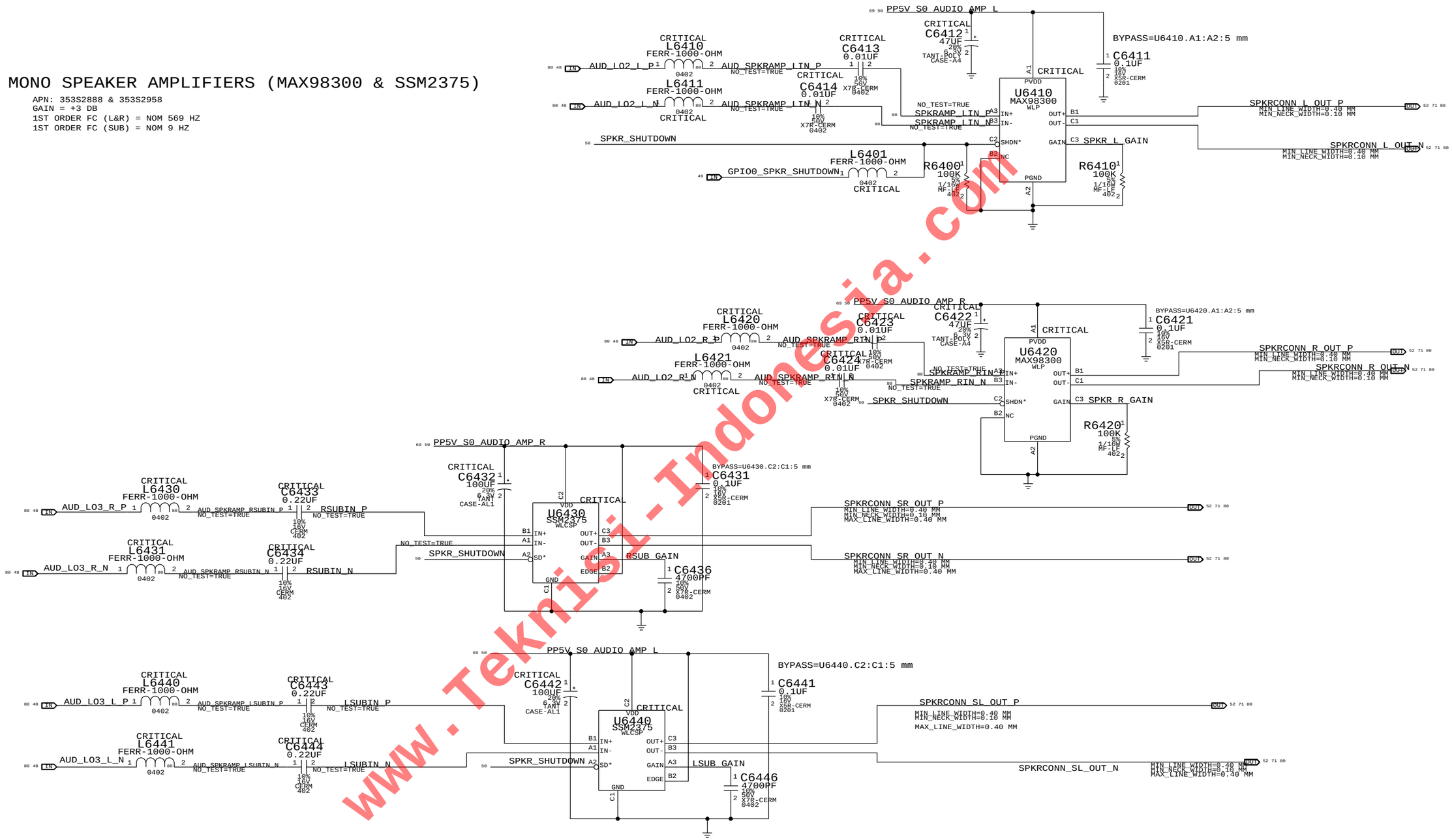
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



Placement Note: Place C6447 and C6452 near U6420

NC C6447 0.0022UF 10% 50V CERM-X7R 0603 NC

NC C6452 0.0022UF 10% 50V CERM-X7R 0603 NC

Placement Note: Place C6448 and C6449 near U6430

NC C6448 0.0022UF 10% 50V CERM-X7R 0603 NC

NC C6449 0.0022UF 10% 50V CERM-X7R 0603 NC

Placement Note: Place C6450 near U6410

NC C6450 0.0022UF 10% 50V CERM-X7R 0603 NC

Placement Note: Place C6451 near U6440

NC C6451 0.0022UF 10% 50V CERM-X7R 0603 NC

BOM_COST_GROUP=AUDIO

SYNC MASTER=DIRK_J44 SYNC DATE=01/09/2013

PAGE TITLE
Audio: Speaker Amps

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 64 OF 120
SHEET 50 OF 82

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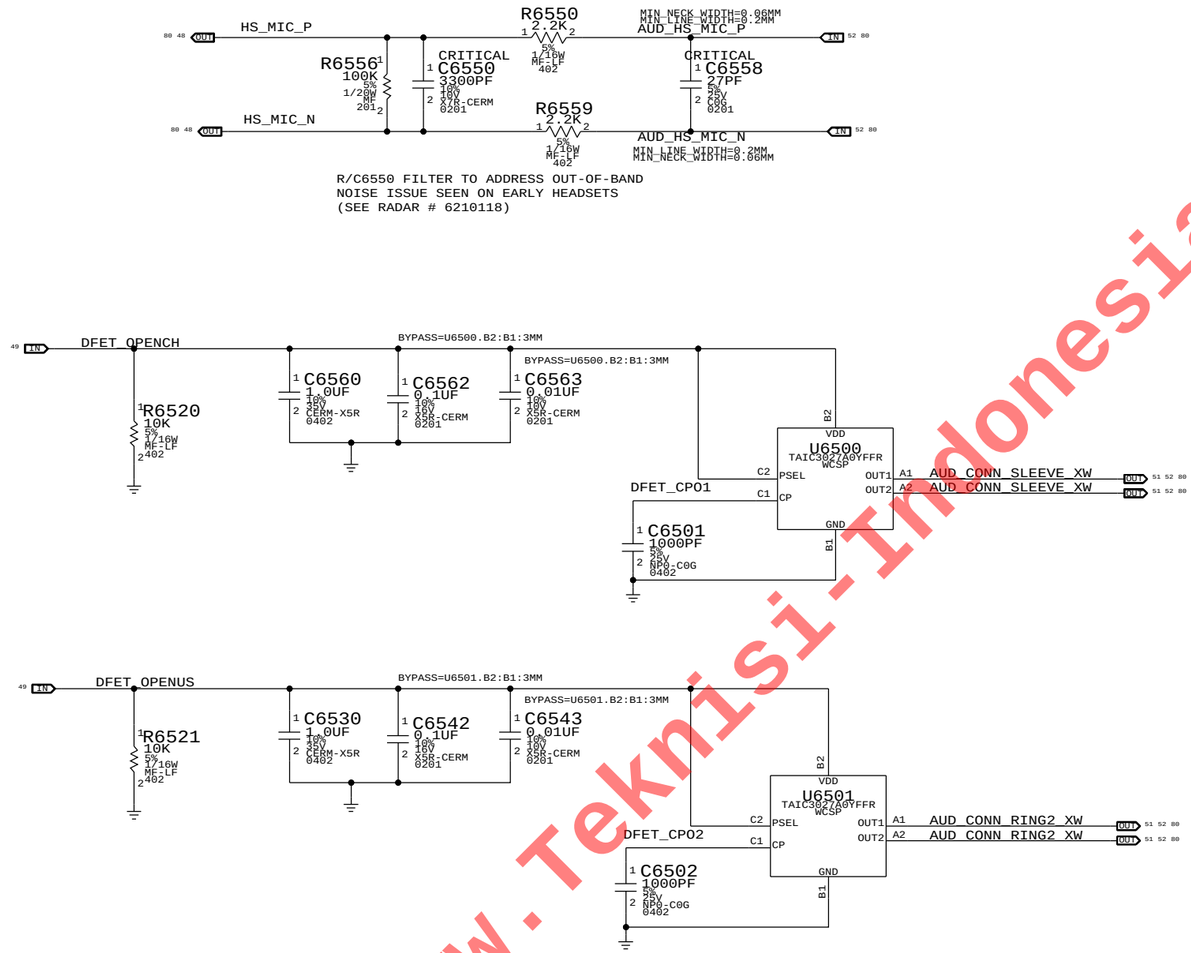

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BOM_COST_GROUP=AUDIO

SYNC MASTER=JCURCIO J44 SYNC DATE=07/25/2013

PAGE TITLE
Audio: Jack Support

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 65 OF 120

SHEET 51 OF 82

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETs OPEN

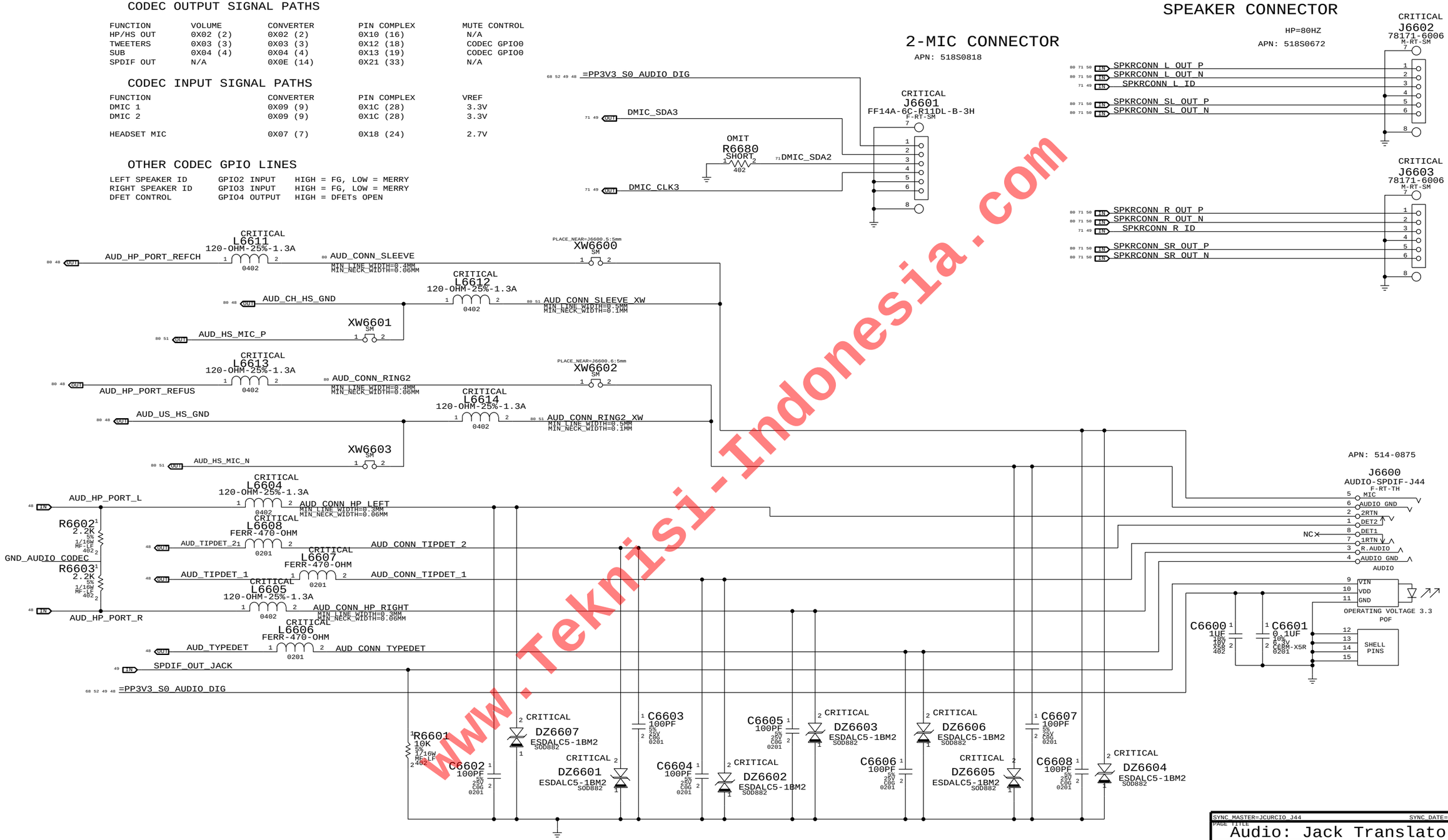
2-MIC CONNECTOR

APN: 518S0818

SPEAKER CONNECTOR

HP=80HZ

APN: 518S0672



BOM_COST_GROUP=AUDIO

SYNC_MASTER=JCURCIO_J44 SYNC_DATE=05/13/2013

PAGE TITLE

Audio: Jack Translators

Apple Inc.

DRAWING NUMBER	051-1573
SIZE	D
REVISION	8.0.0
BRANCH	dvt1
PAGE	66 OF 120
SHEET	52 OF 82

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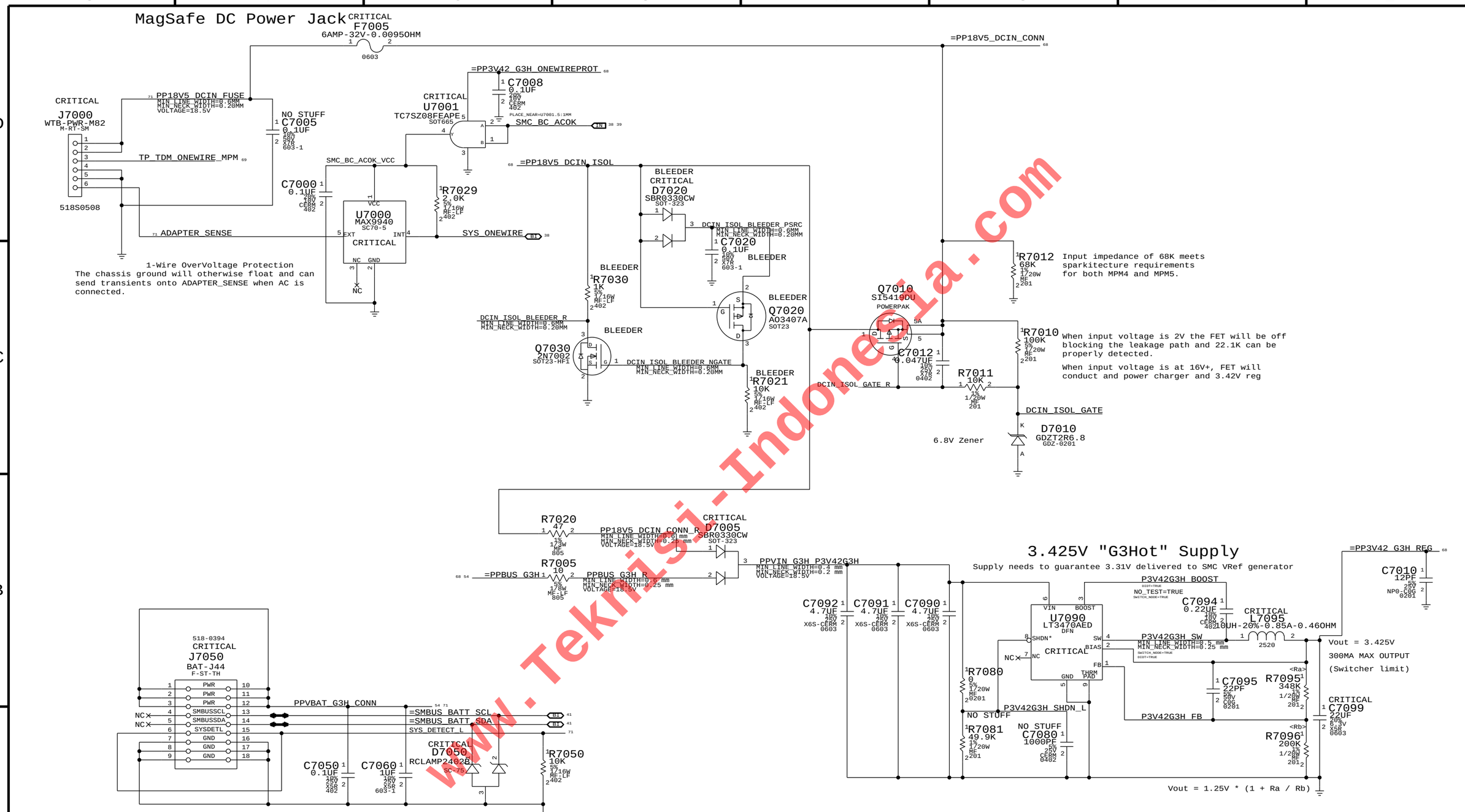

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BOM_COST_GROUP=POWER

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER	051-1573
SIZE	D
REVISION	8.0.0
BRANCH	dvt1
PAGE	70 OF 120
SHEET	53 OF 82

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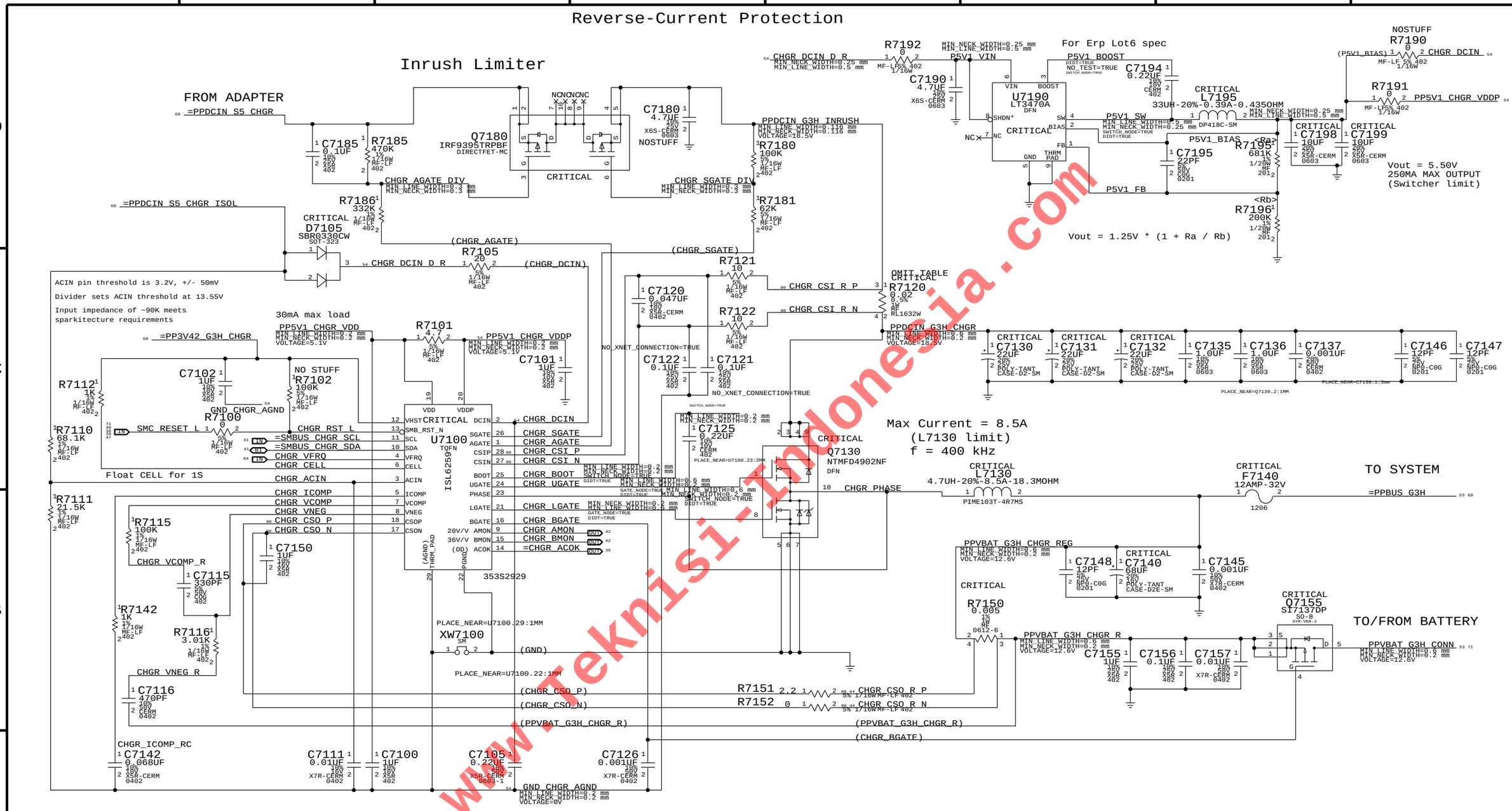

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0387	1	RES,MTL FILM,1W,20MOHM,0.5%,0612,LF,BLK	R7120	CRITICAL	

BOM_COST_GROUP=POWER

SYNC MASTER=AHARTMAN_J52 SYNC DATE=11/06/2013

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 71 OF 120
SHEET 54 OF 82

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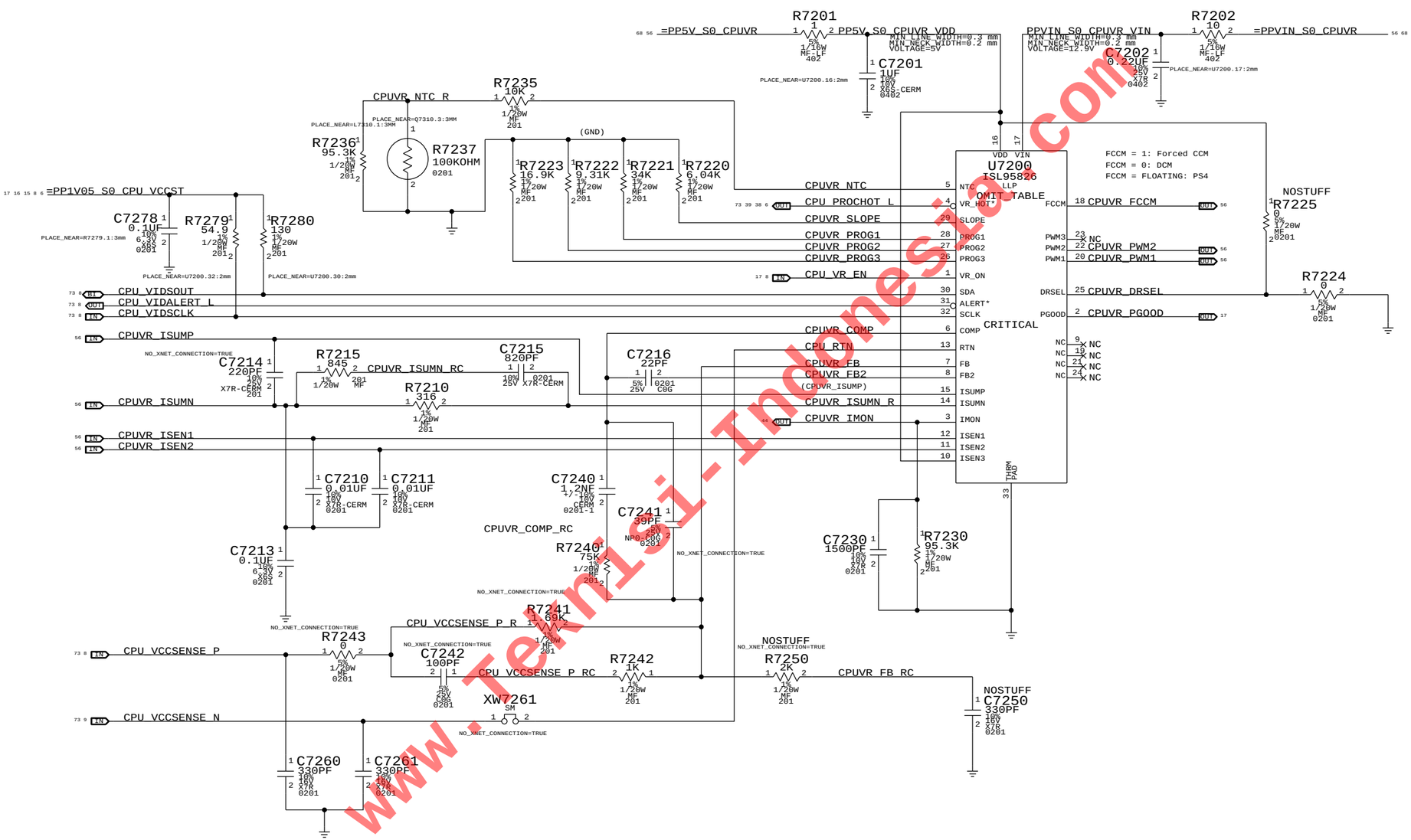
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00036	1	IC,ISL95826AS2378,PWM,PG,VR12.5/6,QFN-32	U7200	CRITICAL	



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BOM_COST_GROUP=POWER

SYNC MASTER=J41 SYNC DATE=10/23/2012

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 72 OF 120

SHEET 55 OF 82

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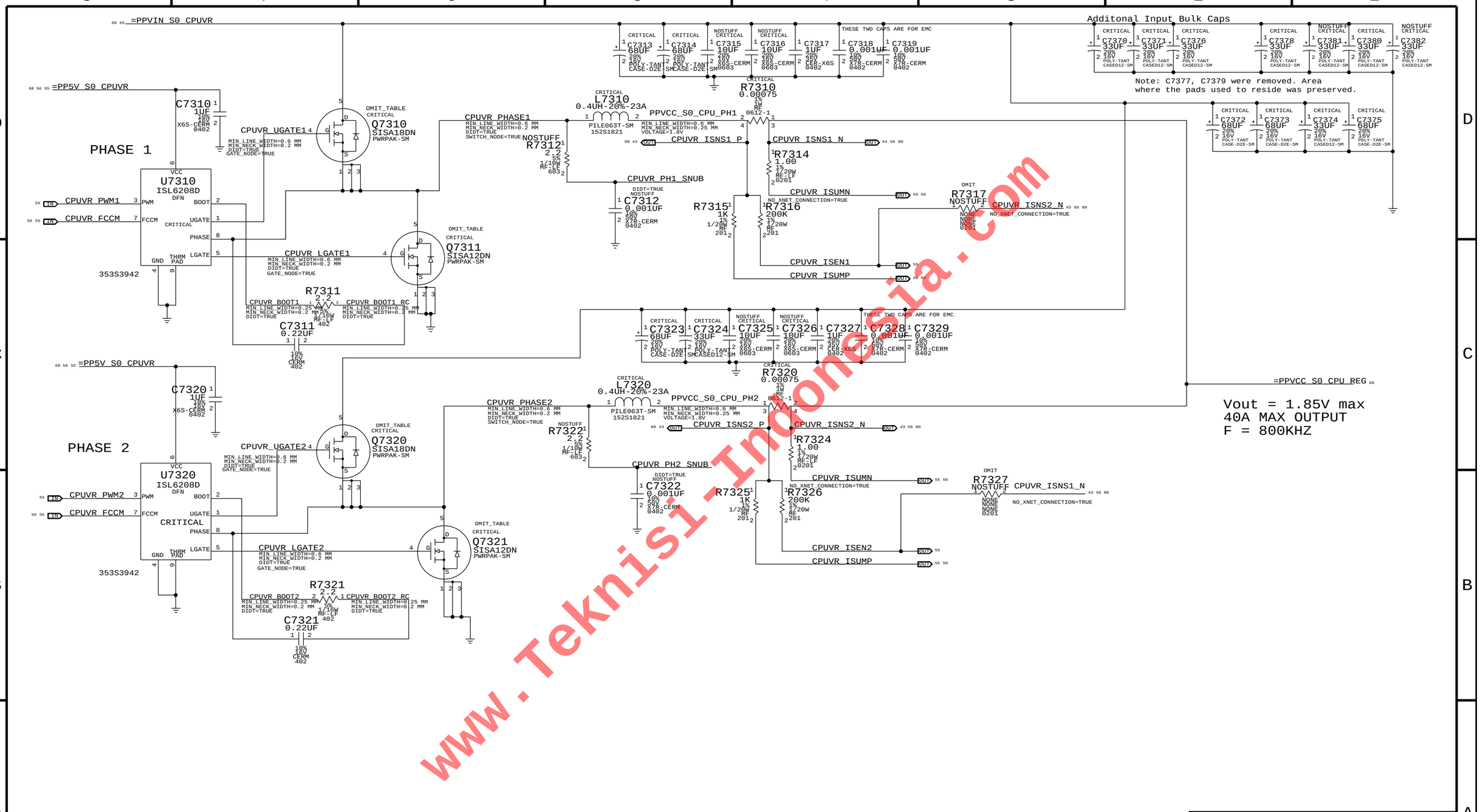

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SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE
CPU VR12.6 VCC Power Stage

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 73 OF 120

SHEET 56 OF 82

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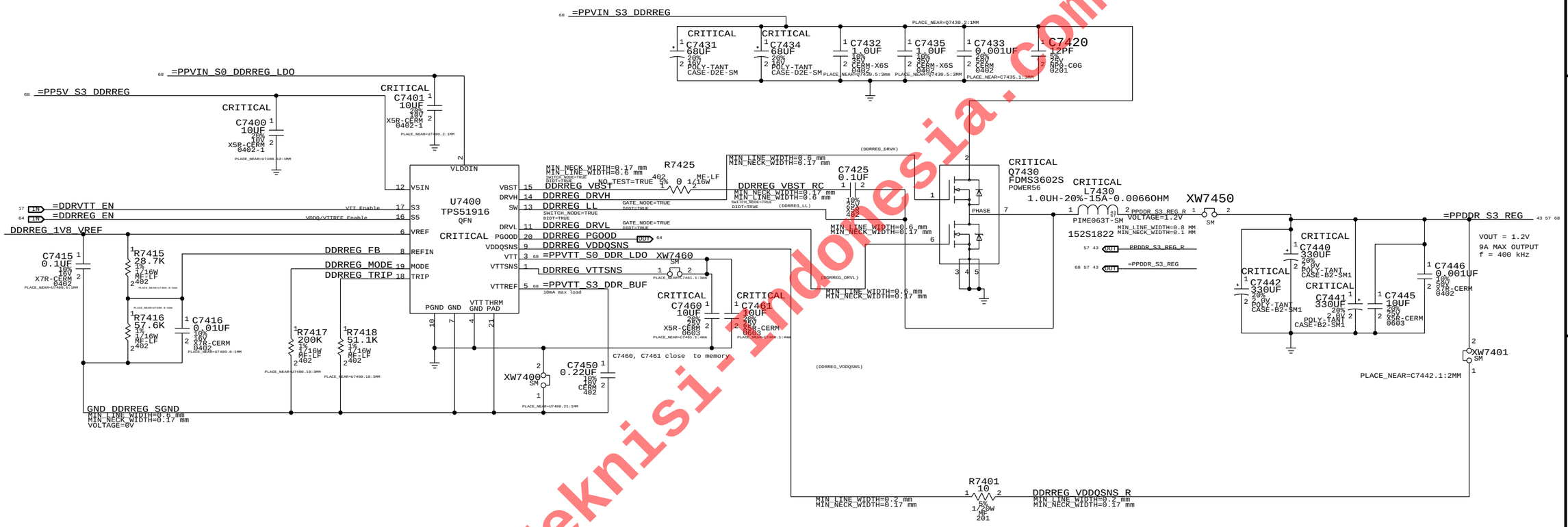
1.2V S3 Regulator



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SYNC_MASTER=J41_MLB SYNC_DATE=05/21/2013

PAGE TITLE
LPDDR3 Supply

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 74 OF 120
SHEET 57 OF 82

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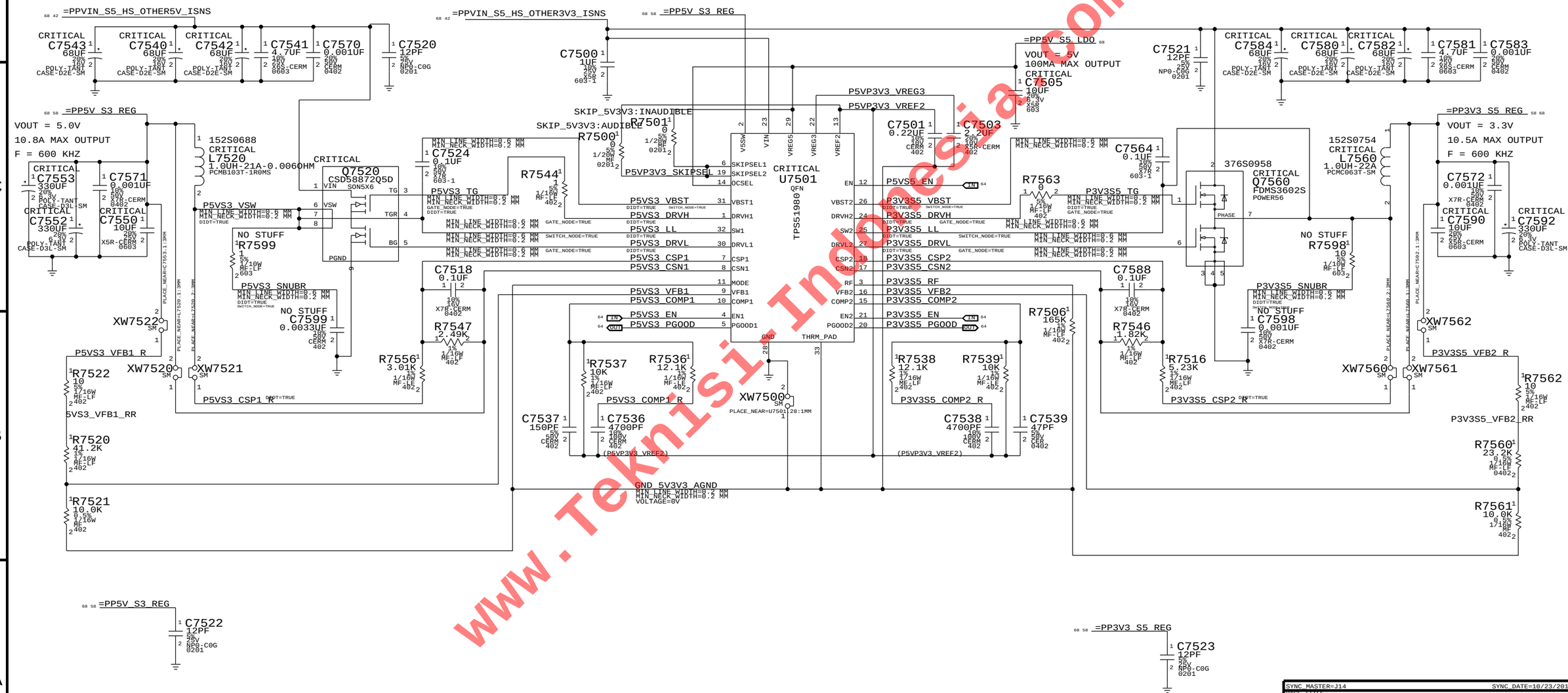
BOM_COST_GROUP=POWER



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SYNC MASTER=J14 SYNC DATE=10/23/2012

PAGE TITLE

5V & 3.3V Power Supply

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 75 OF 120

SHEET 58 OF 82

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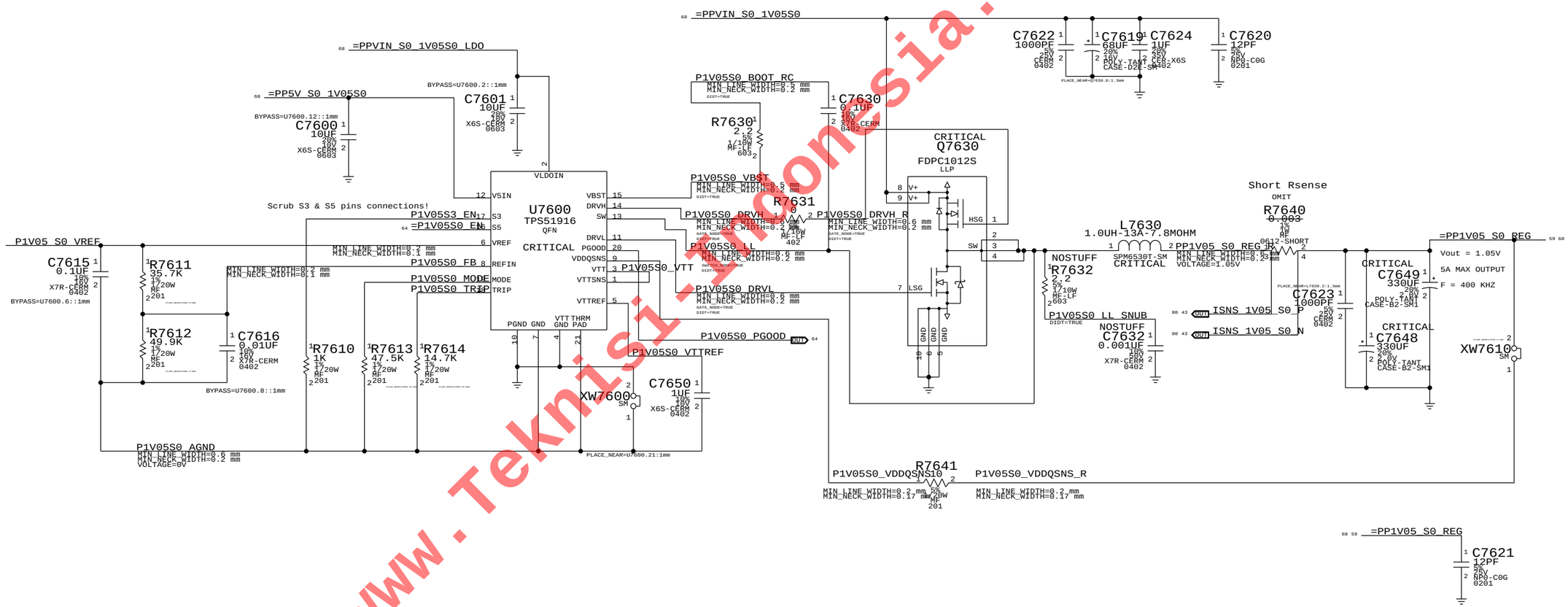
1.05V S0 Regulator



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BOM_COST_GROUP=POWER

SYNC MASTER=AHARTMAN_J52 SYNC DATE=10/29/2013

PAGE TITLE
1.05V Power Supply

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 76 OF 120

SHEET 59 OF 82

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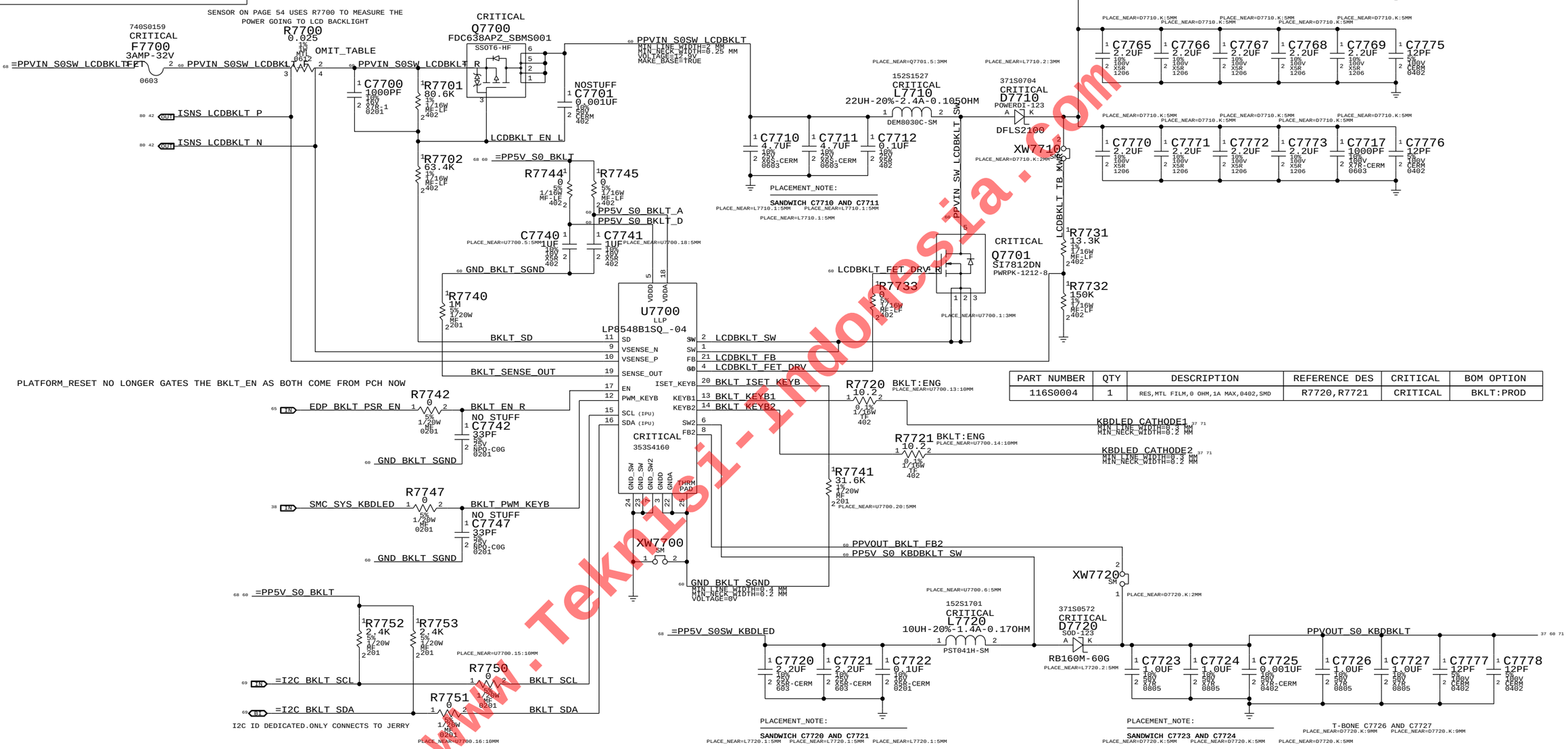
Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)
- =PP5V_S0SW_KBDLED (5V KEYBOARD BACKLIGHT INPUT)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0386	1	RES,MTL FILM,1W,25MOHM,1%,4TERM,0612,BLK	R7700	CRITICAL	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PBUS LINE WIDTHS

- PP5V_S0_BKLT_A — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=5V
- PP5V_S0_BKLT_D — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=5V
- PPVIN_S0SW_LCDBKLT_F — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT_R — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT_FET — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.9V

LCD BKLT LINE WIDTHS

- LCDBKLT_FET_DRV_R — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=5V, GATE_NODE=TRUE, DIDT=TRUE
- LCDBKLT_FET_DRV — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=5V, GATE_NODE=TRUE, DIDT=TRUE
- LCDBKLT_SW — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=53V, SWITCH_NODE=TRUE, DIDT=TRUE
- PPVIN_SW_LCDBKLT_SW — MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=53V, SWITCH_NODE=TRUE, DIDT=TRUE
- PPVOUT_S0_LCDBKLT — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=53V
- PPVOUT_BKLT_FB — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=53V

KBD BKLT LINE WIDTHS

- PP5V_S0_KBDBKLT_SW — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=40V, SWITCH_NODE=TRUE, DIDT=TRUE
- PPVOUT_S0_KBDBKLT — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=40V
- PPVOUT_BKLT_FB2 — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=40V

BOM_COST_GROUP=DISPLAY

SYNC MASTER=SHART J44 SYNC DATE=11/20/2013

PAGE TITLE
LCD & KBD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 77 OF 120
SHEET 60 OF 82

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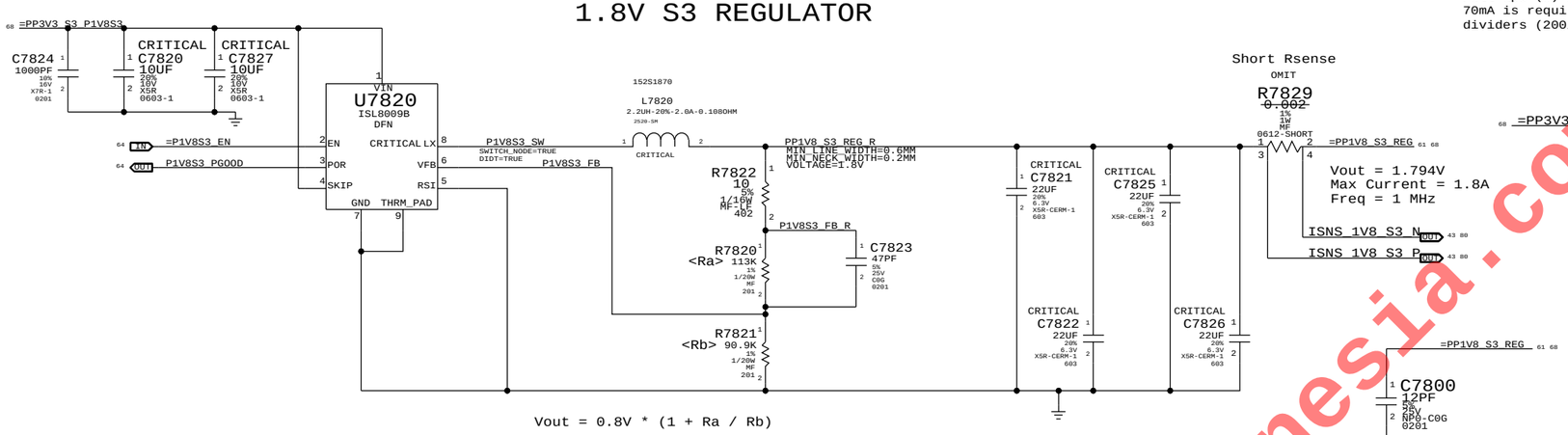
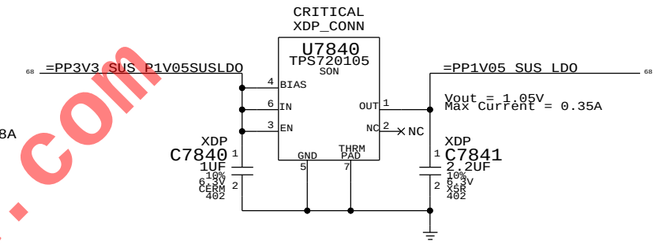
1.8V S3 REGULATOR



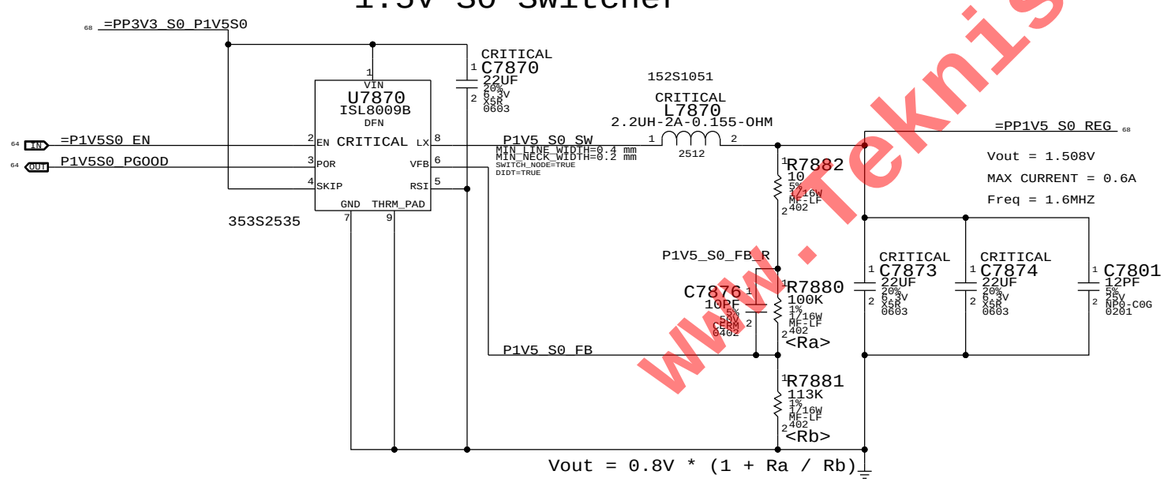
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 Switcher



Vout = 0.8V * (1 + Ra / Rb)

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BOM_COST_GROUP=POWER

SYNC MASTER=AHARTMAN_J52 SYNC DATE=11/06/2013

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 78 OF 120

SHEET: 61 OF 82

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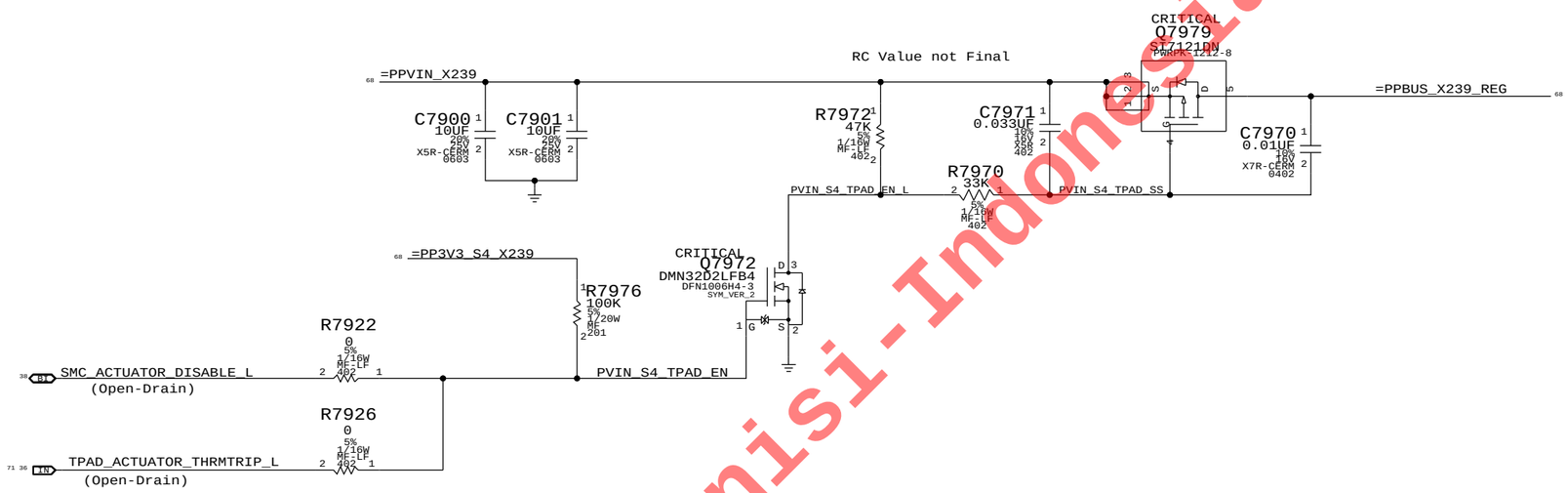

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BOM_COST_GROUP=TRACKPAD

SYNC_MASTER=AHARTMAN_J52 SYNC_DATE=11/06/2013

PAGE TITLE
X239 Power Supply

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

PAGE 79 OF 120

SHEET 62 OF 82

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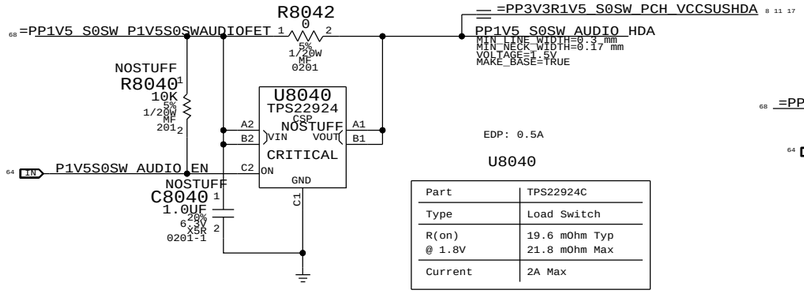
Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

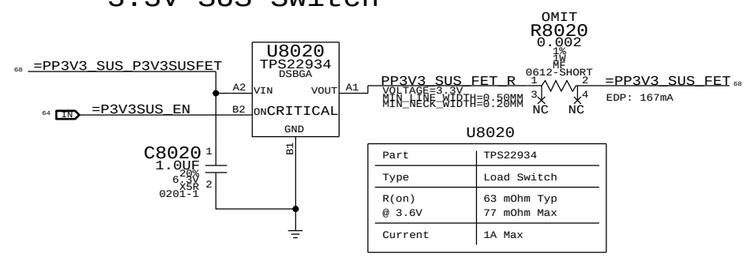
1.5V S0 Audio Switch (BYPASSED)



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

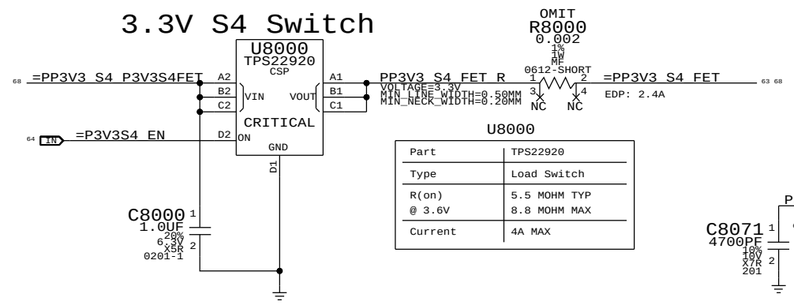
3.3V SUS Switch



U8020

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

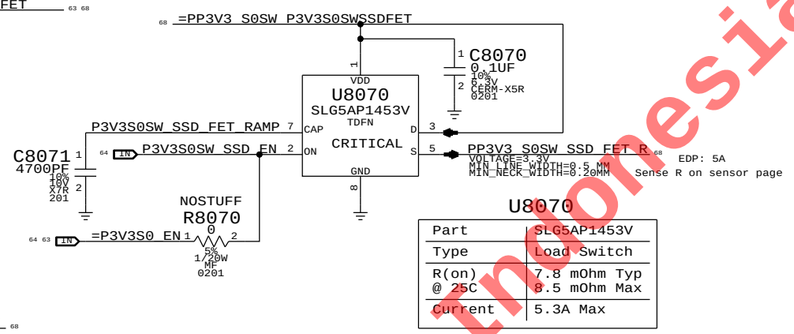
3.3V S4 Switch



U8000

Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.5 MOHM TYP 8.8 MOHM MAX
Current	4A MAX

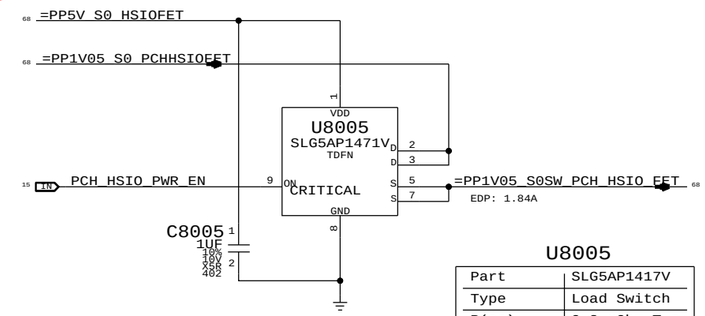
3.3V SSD Switch



U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

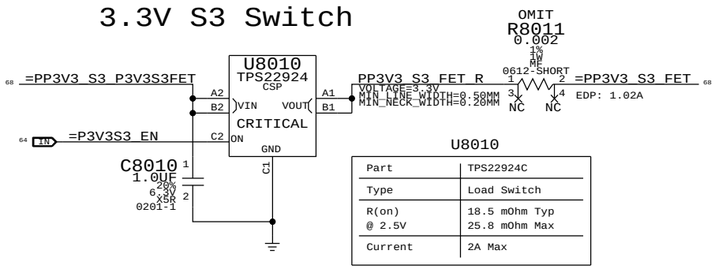
1.05V PCH HSIO Switch



U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

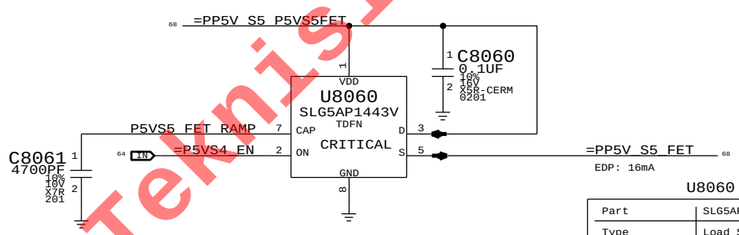
3.3V S3 Switch



U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S4 Switch

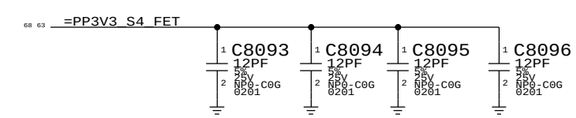


U8060

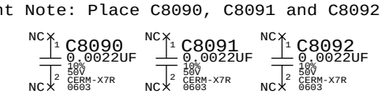
Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

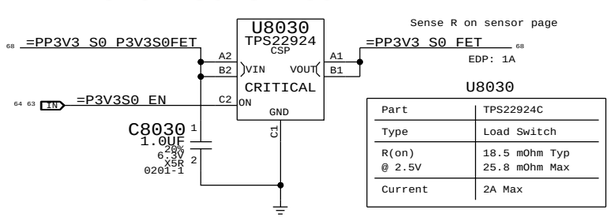
CAPACITORS ADDED FOR NOISE FLOOR REASONS:



Placement Note: Place C8090, C8091 and C8092 near U8000



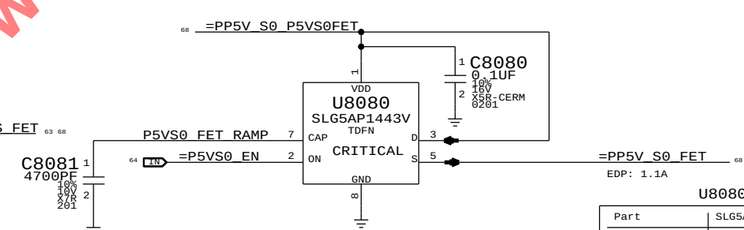
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

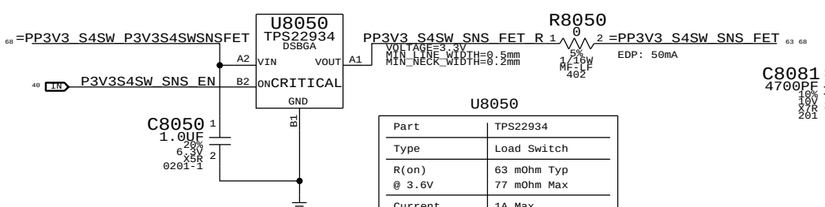
5V S0 Switch



U8080

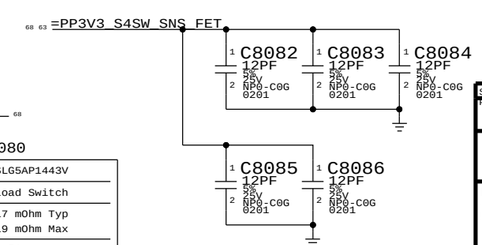
Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

3.3V Sensor Switch



U8050

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max



BOM_COST_GROUP=POWER

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

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SHEET 63 OF 82

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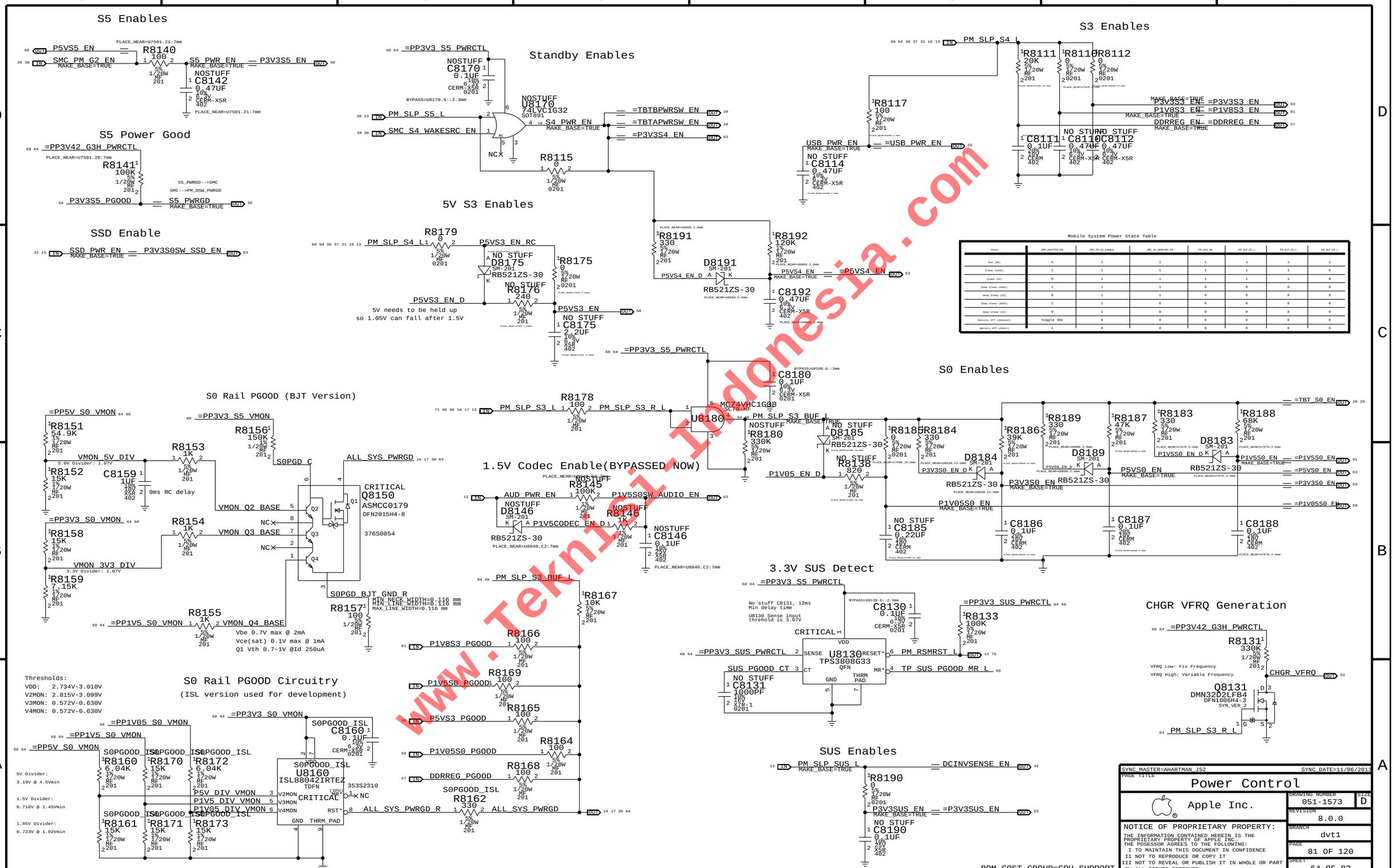

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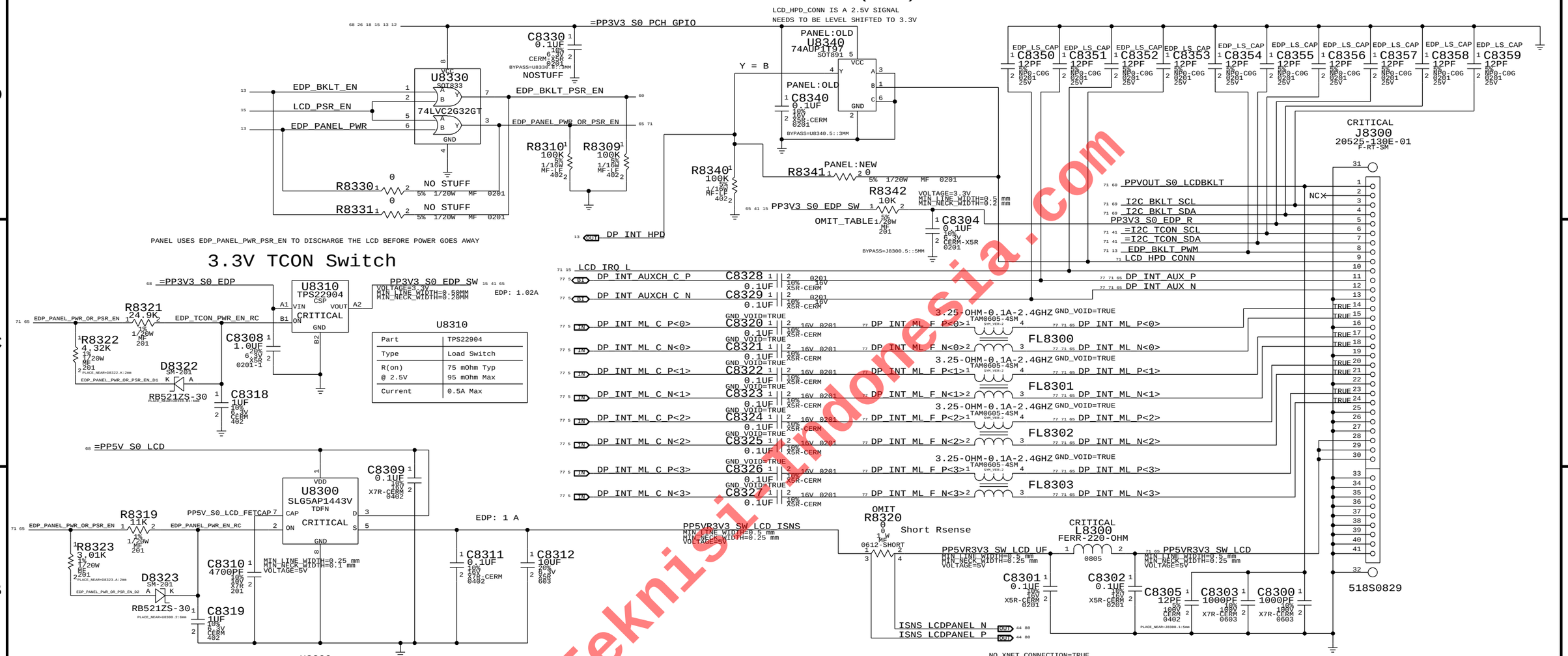
LCD PANEL INTERFACE (eDP)



LCD Panel AUX strapping

S0 Enables

PANEL COMPATIBILITY

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0007	1	RES,MF,1/20W,10K OHM,5,0201,SMD	R8342	CRITICAL	PANEL:OLD
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R8342	CRITICAL	PANEL:NEW

SYNC_MASTER=GKOO_J52 SYNC_DATE=05/04/2014

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 83 OF 120

SHEET: 65 OF 82

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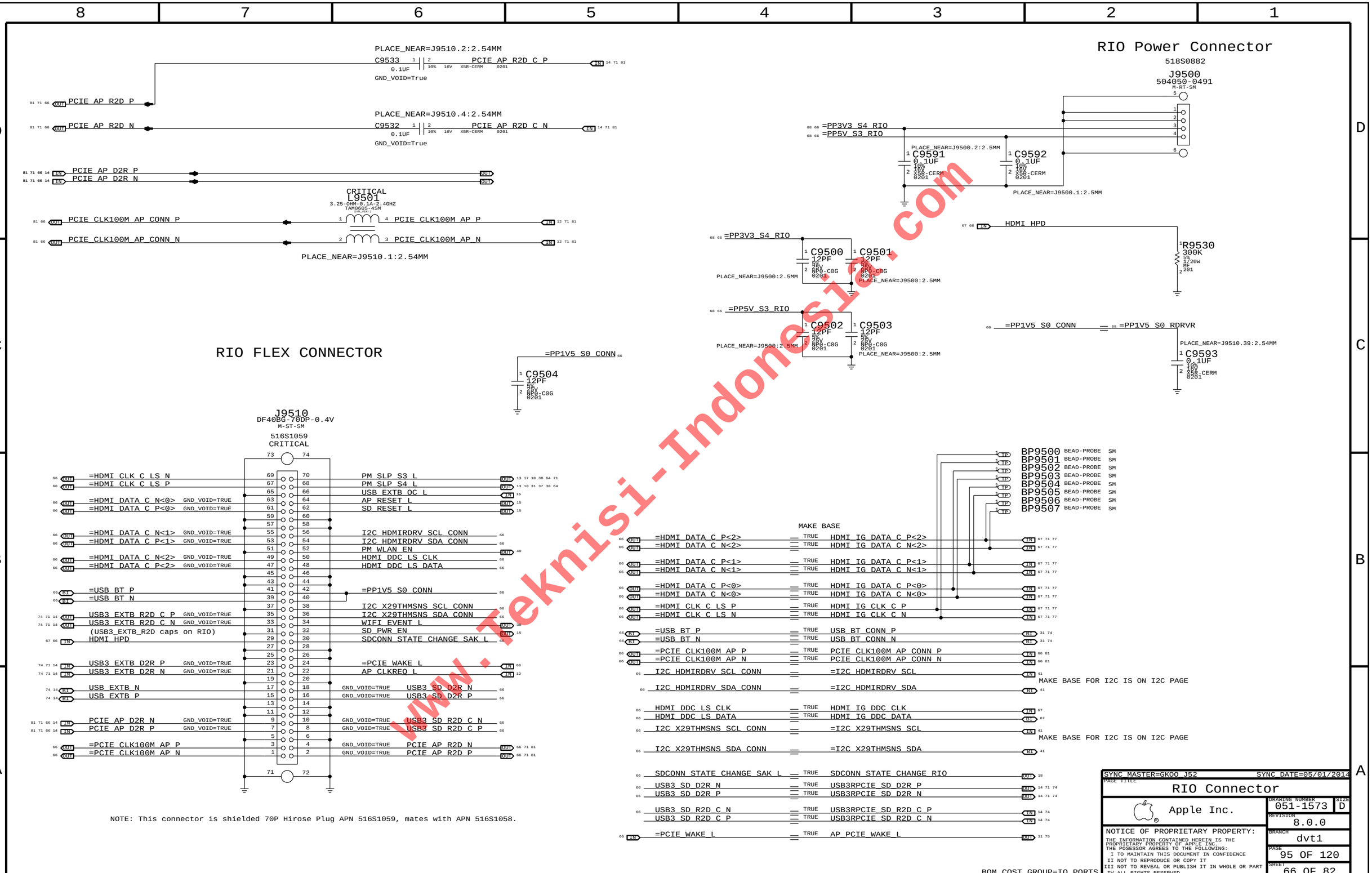

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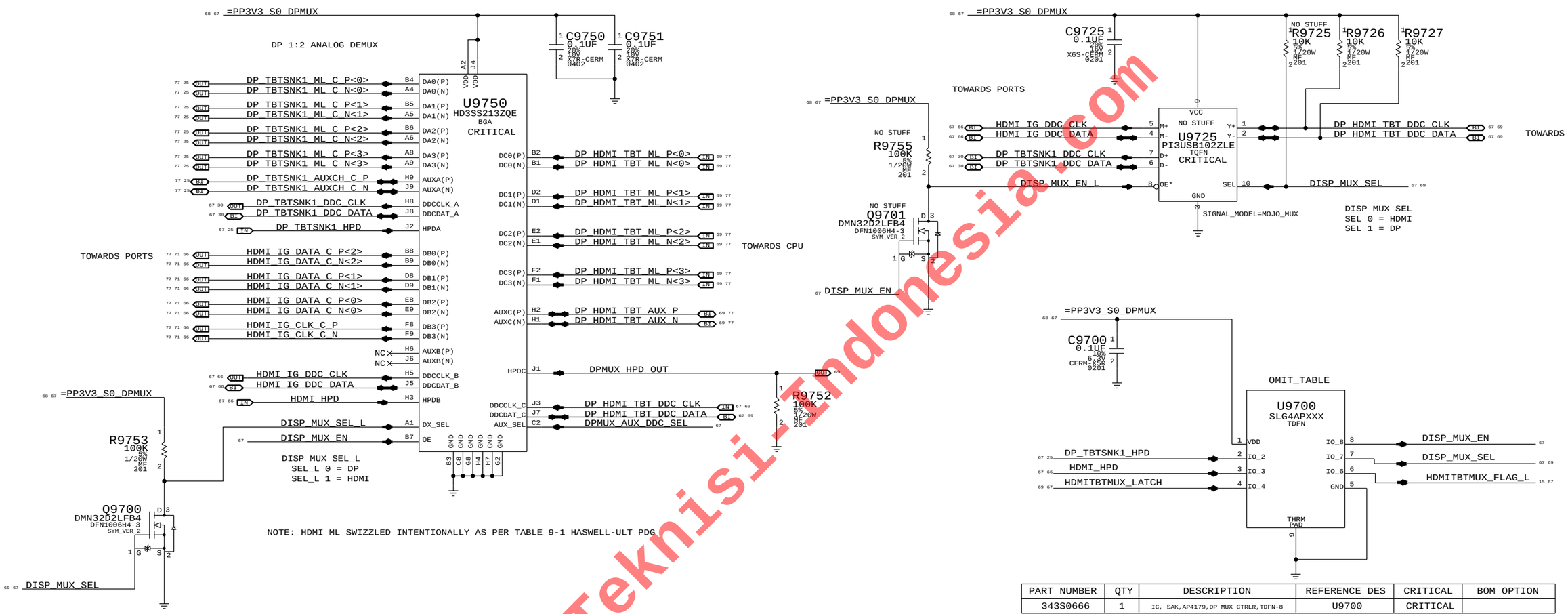
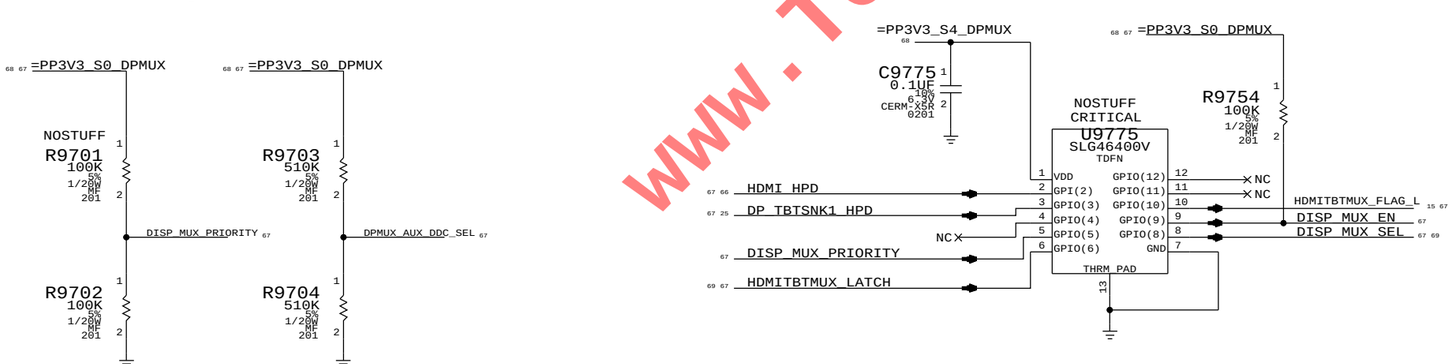
DISPLAY MUX: DP OR HDMI



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0666	1	IC, SAK,AP4179,DP MUX CTRLR,TDFN-8	U9700	CRITICAL	



BOM_COST_GROUP=TBT

SYNC_MASTER=SRAMAN_J44 SYNC_DATE=01/29/2013

PAGE TITLE: Display Mux: HDMI vs DP

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 97 OF 120

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"G3Hot" (Always-Present) Rails

54 53 =PPBUS_G3H — PPBUS_G3H
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE
- =PPVIN_S0SW_LCDBKLTFET 60
- =PPBUS_S0_VSENSE 42
- =PPVIN_SW_TBTBST 27
- =PPVIN_S5_HS_COMPUTING_ISNS_R 42
- =PPVIN_S5_HS_OTHER5V_ISNS_R 42
- =PPVIN_S5_HS_OTHER3V3_ISNS_R 42
- =PPVIN_X239 62

42 =PPVIN_S5_HS_COMPUTING_ISNS — PPBUS_S5_HS_COMPUTING
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE
- =PPVIN_S0_CPUVR 55 56
- =PPVIN_S3_DDRREG 57
- =PPVIN_S0_1V05S0 59

58 42 =PPVIN_S5_HS_OTHER5V_ISNS — PPBUS_S5_HS_OTHER5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V MAKE_BASE=TRUE

58 42 =PPVIN_S5_HS_OTHER3V3_ISNS — PPBUS_S5_HS_OTHER3V3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V MAKE_BASE=TRUE

62 =PPBUS_X239_REG — PPBUS_S4_X239
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=12.3V MAKE_BASE=TRUE
- =PPVIN_X239_PBUS_ISNS_R 42

42 =PPVIN_X239_PBUS_ISNS — PPVIN_S4_TPAD
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V MAKE_BASE=TRUE
- =PPVIN_S4_TPAD 36 71

53 =PP18V5_DCIN_ISOL — PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.5 MM
VOLTAGE=18.5V MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR_ISOL 54
- =PPDCIN_S5_VSENSE 42

53 =PP18V5_DCIN_CONN — PPDCIN_G3H 71
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR 54

53 =PP3V42_G3H_REG — PP3V42_G3H 71
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_G3H_T112 47
- =PP3V3_S5_SMC 38 39 40
- =PP3V42_G3H_HALL 40
- =PP3V42_G3H_CHGR 54
- =PP3V42_G3H_PWRCTL 64
- =PP3V42_G3H_SMBUS_SMC_5 41
- =PP3V42_G3H_SMCUSBMUX 35
- =PP3V42_G3H_TPAD 36
- =PPVIN_S5_SMCVREF 39
- =PPVBAT_G3H_SYSCLK 17
- =PP3V42_G3H_ONEWIREPROT 53
- =PP3V42_G3H_SSDSAK 32
- =PP3V42_G3H_CSPWRGD 17
- =PP3V42_G3H_X239_COFET_EN

17 =PPVRTC_G3_OUT — PPVRTC_G3H
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE
- =PPVRTC_G3_PCH 8 12 13

5V Rails

58 =PP5V_S5_LDO — PP5V_S5 71
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_P5VS5FET 63

63 =PP5V_S5_FET — PP5V_S4
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S4_TPAD 36

58 =PP5V_S3_REG — PP5V_S3 71
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_ALSCAM 34
- =PP5V_S3_LTUSB 35
- =PP5V_S3_RIO 66
- =PP5V_S0_P5VS0FET 63
- =PP5V_S0_1V05S0 59
- 48 =PP5V_S3_AUDIO — =PP5V_S0_AUDIO_AMP 69
- =PP5V_S0_LCD 65
- =PP5V_S3_DDRREG 57

43 =PP5V_S0_ISNS — PP5V_S0 71
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_LPCPLUS
- =PP5V_S0_CPUVR 55 56
- =PP5V_S0_VMON 64
- =PP5V_S0_PCH_STRAP 17
- =PP5V_S0_XDPJTAGISOL 16
- =PP5V_S0_FAN 46
- =PP5V_S0_BKLT 60
- =PP5V_S0SW_KBDLED 60
- =PP5V_S0_ALSCAM 34
- =PP5V_S0_HSIOFET 63

3.3V Rails

58 =PP3V3_S5_REG — PP3V3_S5 71 80
MIN_LINE_WIDTH=0.2 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S0SW_P3V3S0SWSSDFET 63
- =PP3V3_S4_TBTBPWRSW 29
- =PP3V3_S0_P3V3S0FET 63
- =PP3V3_S3_P3V3S3FET 63
- =PP3V3_S4_P3V3S4FET 63
- =PP3V3_S5_DBGLEDS 18
- =PP3V3_SUS_P3V3SUSFET 63
- =PP3V3_S5_CSPWRGD 17
- =PP3V3_S5_PCH_VCCDSW 8 11
- =PP3V3_S5_PWRCTL 64
- =PP3V3_S5_SYSCLK 17 18
- =PP3V3_S5_VMON 64
- =PP3V3_S5_PCH_GPIO 13 15
- =PP3V3_S4_TBTAPWRSW 28
- =PP3V3_S4SW_P3V3S4SWSNSFET 63
- =PP3V3_S5_XDPJTAGISOL 16
- =PP3V3_S0_P1V5S0 61
- =PP3V3_S5_WLAN 31
- =PP3V3_S5_CAMPWREN
- =PP3V3_S3_P1V8S3 61

63 =PP3V3_S4_FET — PP3V3_S4 71
MIN_LINE_WIDTH=0.20MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S4_SMC 18 39 40
- =PP3V3_S4_TPAD 36 37 71
- =PP3V3_S4_BT 31
- =PP3V3_S4_TBT_ISNS_R 44
- =PP3V3_S4_DPMUX 67
- =PP3V3_S4_RIO 66
- =PP3V3_S4_X239 62
- =PP3V3_S4_SMBUS_SMC_2 41
- =PP3V3_S4_CAMPWREN 18

63 =PP3V3_SUS_FET — PP3V3_SUS
MIN_LINE_WIDTH=0.20MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_SUS_ROM 47
- =PP3V3_SUS_PCH_VCCSUS_GPIO 8 11
- =PP3V3_SUS_PCH_VCCSUS_ICC 8
- =PP3V3_SUS_PCH_VCC_SPI 8 11 14
- =PP3V3_SUS_PWRCTL 64
- =PP3V3_SUS_P1V05SUSLDO 61
- =PP3V3_SUS_PCH_GPIO 14
- =PP3V3_SUS_PCH_VCCSUS_RTC 8 11

63 =PP3V3_S3_FET — PP3V3_S3 71
MIN_LINE_WIDTH=0.20MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S3SW_SD_RESET 15
- =PP3V3_S3_PCH_GPIO 15
- =PP3V3_S3_SDBUF 18
- =PP3V3_S3RS4_PCH_GPIO 15
- =PP3V3_S3_SYSCLKGEN 18
- =PP3V3_S3_CAMERA_R 44
- =PP3V3_S3_TPAD

43 =PP3V3_S0_ISNS — PP3V3_S0 71 80
MIN_LINE_WIDTH=0.2 mm VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20mm MAKE_BASE=TRUE
- =PP3V3_S0_FAN 46
- =PP3V3_S0_SMBUS_SMC_0 41
- =PP3V3_S0_PCH_VCC3_3_GPIO 8 11
- =PP3V3_S0_PCH_GPIO 12 13 15 18 26 65
- =PP3V3_S0_CPUTHMSNS 44 45
- 48 =PP3V3_S0_AUDIO — =PP3V3_S0_TBTTHMSNS 45
- 52 49 48 =PP3V3_S0_AUDIO_DIG — =PP3V3_S0_PCH_VCCTS 8 11
- 30 =PP3V3_S0_DDCMUX — =PP3V3_S0_RSTBUF 18
- 67 =PP3V3_S0_DPMUX — =PP3V3_S0_SB_PM 17
- 65 =PP3V3_S0_EDP — =PP3V3_S0_SMBUS_PCH 41
- =PP3V3_S0_LCD 65
- =PP3V3_S0_SMBUS_SMC_1 41
- =PP3V3_S0_SMC 39
- =PP3V3R1V8_S0_PCH_VCCSDIO 8 11 40
- =PP3V3_S0_VMON 64
- =PP3V3_S0RTBTLC_PCH_GPIO 15
- =PP3V3_S0_SYSCLKGEN 18
- =PP3V3_S0_OOB1_PWRDN 32
- =PP3V3_S0_MEM_VTTPWRCTL 17
- =PP3V3_S0_SNS_BMON 44
- =PP3V3_S0_HS_COMPUTING_ISNS 42 43
- =PP3V3_S0_VRISNS 43
- =PP3V3_S0_CAMERA_R 44
- =PP3V3_S0_SMBUS_SMC_3 41
- =PP3V3_S0_TPAD 37

63 =PP5V_S0_FET — PP5V_S0_FET
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_ISNS_R 43

63 =PP3V3_S0_FET — PP3V3_S0_FET
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S0_ISNS_R 43

19 PPVREF_S3_MEM_VREFDQ_A — PP0V6_S3_MEM_VREFDQ_A 20 21 76
MAKE_BASE=TRUE VOLTAGE=0.6V
68 19 PPVREF_S3_MEM_VREFCA — PP0V6_S3_MEM_VREFCA_A 20 21 76
MAKE_BASE=TRUE VOLTAGE=0.6V
19 PPVREF_S3_MEM_VREFDQ_B — PP0V6_S3_MEM_VREFDQ_B 22 23 76
MAKE_BASE=TRUE VOLTAGE=0.6V
68 19 PPVREF_S3_MEM_VREFCA — PP0V6_S3_MEM_VREFCA_B 22 23 76
MAKE_BASE=TRUE VOLTAGE=0.6V

63 =PP3V3_S4SW_SNS_FET — PP3V3_S4SW_SNS
MIN_LINE_WIDTH=0.20MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S4_HS_OTHER_ISNS 42
- =PP3V3_S4_ISNS 42 43 44

63 PP3V3_S0SW_SSD_FET_R — PP3V3_S0SW_SSD_FET
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S0SW_SSD_ISNS_R 43

43 =PP3V3_S0SW_SSD_ISNS — PP3V3_S0SW_SSD
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S0SW_SSD 32

44 =PP3V3_S4_TBT_ISNS — PP3V3_S4_TBT
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S4_TBT 25 26 27

1.5V/1.2V/1.8V/1.05V RAILS

43 =PP1V2_S3_CPUDDR_ISNS — PP1V2_S3_CPUDDR 76
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
MAKE_BASE=TRUE
- =PPVMEMIO_S0_CPU 8 10

57 43 =PPDDR_S3_REG — PP1V2_S3 76
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
- =PP1V2_S3_MEM_VDDQ 20 21 22 23
- =PPVIN_S0_DDRREG_LDO 57
- =PP1V2_S3_CPUDDR_ISNS_R 43
- =PP1V2_S3_MEM_VTTPWRCTL 17
- =PPDDR_S3_MEMVREF 19
- =PP1V2_S3_MEM_VDDCA 20 21 22 23
- =PP1V2_S3_MEM_VDD2 20 21 22 23

61 =PP1V8_S3_REG — PP1V8_S3
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S3_MEM 20 21 22 23

57 =PPVTT_S0_DDR_LDO — PP0V6_S0_DDRVTT 71 76
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.6V
MAKE_BASE=TRUE
- =PP0V6_S0_MEM_VTT_A 24
- =PP0V6_S0_MEM_VTT_B 24

57 =PPVTT_S3_DDR_BUF — PPVTTDDR_S3 71 76
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.6V
MAKE_BASE=TRUE

61 =PP1V05_SUS_LDO — PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_SUS_PCH_JTAG 16

61 =PP1V5_S0_REG — PP1V5_S0 71
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S0SW_P1V5S0SWAUDIOFET 63
- =PP1V5_S0_PCH_VCCTS 8
- =PP1V5_S0_AUDIO 49
- =PP1V5_S0_VMON 64
- =PP1V5_S0_RDRVR 66

59 =PP1V05_S0_REG — PP1V05_S0 71
? mA
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0M_PCH_VCCASW 8 11
- =PP1V05_S0_PCH_VCC 8 11
- =PP1V05_S0_PCHHSIOFET 63
- =PP1V05_S0_PCH_PLLFILTERS 11
- =PP1V05_S0_VMON 64
- =PP1V05_S0_PCH_VCCIO_USB2 8 11
- =PP1V05_S0_PCH_VCCCLK 8 11
- =PP1V05_S0_CPU_VCCST 6 8 15 16 17 55
- =PP1V05_S0_PCH_VCCIO_HSIO 8
- =PPVIN_S0_1V05S0_LDO 59
- =PP1V05_S0_SMC 39
- =PP1V05_S0_XDP 16

63 =PP1V05_S0SW_PCH_HSIO_FET — PP1V05_S0SW_PCH_HSIO
1.84A
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0SW_PCH_VCCHSIO 8 11
- =PP1V05_S0SW_PCH_VCCPLL_HSIO 11

TBT RAILS (OFF WHEN NO CABLE)

PPVIN_SW_TBTBST 27
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

27 =PP15V_TBT_REG — PP15V_TBT
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=15V
MAKE_BASE=TRUE
- =PPHV_S4SW_TBTAPWRSW 28
- =PPHV_S4SW_TBTBPWRSW 29

PP3V3_TBTLC 18 25 26
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PPVDDIO_TBTLC_CLK 17

CPU "VCORE" RAILS

56 =PPVCC_S0_CPU_REG — PPVCC_S0_CPU 71
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PPVCC_S0_CPU 8 10 44

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM

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SYNC_MASTER=SHART_J44 SYNC_DATE=01/14/2013

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Power Aliases

Apple Inc.

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HDMI VS TBT

5	=DP_TBTSNK1_ML_C_P<0>	MAKE_BASE	TRUE	DP_HDMI_TBT_ML_P<0>	67 77
5	=DP_TBTSNK1_ML_C_N<0>		TRUE	DP_HDMI_TBT_ML_N<0>	67 77
5	=DP_TBTSNK1_ML_C_P<1>		TRUE	DP_HDMI_TBT_ML_P<1>	67 77
5	=DP_TBTSNK1_ML_C_N<1>		TRUE	DP_HDMI_TBT_ML_N<1>	67 77
5	=DP_TBTSNK1_ML_C_P<2>		TRUE	DP_HDMI_TBT_ML_P<2>	67 77
5	=DP_TBTSNK1_ML_C_N<2>		TRUE	DP_HDMI_TBT_ML_N<2>	67 77
5	=DP_TBTSNK1_ML_C_P<3>		TRUE	DP_HDMI_TBT_ML_P<3>	67 77
5	=DP_TBTSNK1_ML_C_N<3>		TRUE	DP_HDMI_TBT_ML_N<3>	67 77
13	=DP_TBTSNK1_AUXCH_C_P		TRUE	DP_HDMI_TBT_AUX_P	67 77
13	=DP_TBTSNK1_AUXCH_C_N		TRUE	DP_HDMI_TBT_AUX_N	67 77
13	=DP_TBTSNK1_DDC_CLK		TRUE	DP_HDMI_TBT_DDC_CLK	67
13	=DP_TBTSNK1_DDC_DATA		TRUE	DP_HDMI_TBT_DDC_DATA	67
13	=DP_TBTSNK1_HPD		TRUE	DPMUX_HPD_OUT	67

25	HDMITBTMUX_SEL_TBT (MAKE_BASE=TRUE)		=TBT_GO2SX_BIDIR	15
			DISP_MUX_SEL	67
13	DP_AUXCH_ISOL_L		HDMITBTMUX_LATCH (MAKE_BASE=TRUE)	67

EPD PANEL

60	=I2C_BKLT_SCL	MAKE_BASE	TRUE	I2C_BKLT_SCL	65 71
60	=I2C_BKLT_SDA		TRUE	I2C_BKLT_SDA	65 71

UNUSED SIGNALS

12	TP_PCIE_CLK100M_FWP	MAKE_BASE	TRUE	NO_TEST=TRUE	NC_PCIE_CLK100M_FWP
12	TP_PCIE_CLK100M_FWN		TRUE	NO_TEST=TRUE	NC_PCIE_CLK100M_FWN
14	TP_PCIE_FW_D2RP		TRUE	NO_TEST=TRUE	NC_PCIE_FW_D2RP
14	TP_PCIE_FW_D2RN		TRUE	NO_TEST=TRUE	NC_PCIE_FW_D2RN
14	TP_PCIE_FW_R2D_CP		TRUE	NO_TEST=TRUE	NC_PCIE_FW_R2D_CP
14	TP_PCIE_FW_R2D_CN		TRUE	NO_TEST=TRUE	NC_PCIE_FW_R2D_CN
12	TP_PCIE_CLK100M_ENETSDP		TRUE	NO_TEST=TRUE	NC_PCIE_CLK100M_ENETSDP
12	TP_PCIE_CLK100M_ENETSDN		TRUE	NO_TEST=TRUE	NC_PCIE_CLK100M_ENETSDN
14	USB_IR_P		TRUE	NO_TEST=TRUE	NC_USB_IRP 74
14	USB_IR_N		TRUE	NO_TEST=TRUE	NC_USB_IRN 74
14	TP_USB_CAMERAP		TRUE	NO_TEST=TRUE	NC_USB_CAMERAP 74
14	TP_USB_CAMERAN		TRUE	NO_TEST=TRUE	NC_USB_CAMERAN 74
14	TP_USB_SDP		TRUE	NO_TEST=TRUE	NC_USB_SDP 74
14	TP_USB_SDN		TRUE	NO_TEST=TRUE	NC_USB_SDN 74
12	TP_HDA_SDIN1		TRUE	NO_TEST=TRUE	NC_HDA_SDIN1
13	TP_PCI_PME_L		TRUE	NO_TEST=TRUE	NC_PCI_PME_L
14	TP_CLINK_CLK		TRUE	NO_TEST=TRUE	NC_CLINK_CLK
14	TP_CLINK_DATA		TRUE	NO_TEST=TRUE	NC_CLINK_DATA
14	TP_CLINK_RESET_L		TRUE	NO_TEST=TRUE	NC_CLINK_RESET_L
12	TP_ITPXDP_CLK100MN		TRUE	NO_TEST=TRUE	NC_ITPXDP_CLK100MN
12	TP_ITPXDP_CLK100MP		TRUE	NO_TEST=TRUE	NC_ITPXDP_CLK100MP
12	TP_PCH_I2S1_TXD		TRUE	NO_TEST=TRUE	NC_PCH_I2S1_TXD
12	TP_PCH_I2S1_SFRM		TRUE	NO_TEST=TRUE	NC_PCH_I2S1_SFRM
12	TP_PCH_I2S1_SCLK		TRUE	NO_TEST=TRUE	NC_PCH_I2S1_SCLK
13	TP_PCH_SLP_WLAN_L		TRUE	NO_TEST=TRUE	NC_PCH_SLP_WLAN_L
13	TP_PCH_SLP_LAN_L		TRUE	NO_TEST=TRUE	NC_PCH_SLP_LAN_L
14	TP_SPI_CS1_L		TRUE	NO_TEST=TRUE	NC_SPI_CS1_L
14	TP_SPI_CS2_L		TRUE	NO_TEST=TRUE	NC_SPI_CS2_L
14	TP_USB_5N		TRUE	NO_TEST=TRUE	NC_USB_5N 74
14	TP_USB_5P		TRUE	NO_TEST=TRUE	NC_USB_5P 74
48	TP_AUD_CODEC_MICBIAS1_L		TRUE	NO_TEST=TRUE	NC_AUD_CODEC_MICBIAS1_L
48	TP_AUD_CODEC_MICBIAS1_R		TRUE	NO_TEST=TRUE	NC_AUD_CODEC_MICBIAS1_R
48	TP_AUD_CODEC_MICBIAS2_L		TRUE	NO_TEST=TRUE	NC_AUD_CODEC_MICBIAS2_L
48	TP_AUD_CODEC_MICBIAS2_R		TRUE	NO_TEST=TRUE	NC_AUD_CODEC_MICBIAS2_R
64	TP_SUS_PGOOD_MR_L		TRUE	NO_TEST=TRUE	NC_SUS_PGOOD_MR_L
	TP_SMC_TRST_L		TRUE	NO_TEST=TRUE	NC_SMC_TRST_L
	TP_SMC_MD1		TRUE	NO_TEST=TRUE	NC_SMC_MD1
53	TP_TDM_ONEWIRE_MPM		TRUE	NO_TEST=TRUE	NC_TDM_ONEWIRE_MPM

TBT UNUSED NETS

25	TP_TBT_MONDC0	TRUE	MAKE_BASE=TRUE	NC_TBT_MONDC0
25	TP_TBT_MONDC1	TRUE	MAKE_BASE=TRUE	NC_TBT_MONDC1
25	TP_TBT_PCIE_RESET0_L	TRUE	MAKE_BASE=TRUE	NC_TBT_PCIE_RESET0_L
25	TP_TBT_XTAL25OUT	TRUE	MAKE_BASE=TRUE	NC_TBT_XTAL25OUT
25	TP_DP_TBTSRC_ML_CP<3>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<3>
25	TP_DP_TBTSRC_ML_CN<3>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<3>
25	TP_DP_TBTSRC_ML_CP<2>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<2>
25	TP_DP_TBTSRC_ML_CN<2>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<2>
25	TP_DP_TBTSRC_ML_CP<1>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<1>
25	TP_DP_TBTSRC_ML_CN<1>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<1>
25	TP_DP_TBTSRC_ML_CP<0>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<0>
25	TP_DP_TBTSRC_ML_CN<0>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<0>
25	TP_DP_TBTSRC_AUXCH_CP	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_AUXCH_CP
25	TP_DP_TBTSRC_AUXCH_CN	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_AUXCH_CN

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Digital Ground

68 =PP5V_S0_AUDIO_AMP

XWA202 (SM) 1 2 — PP5V_S0_AUDIO_AMP_L 50
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

XWA203 (SM) 1 2 — PP5V_S0_AUDIO_AMP_R 50
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

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LPDDR3 COMMAND/ADDRESS

		MAKE_BASE			
7	=MEM_A_A<5>		TRUE	MEM_A_CAA<0>	20 24 76
7	=MEM_A_A<9>		TRUE	MEM_A_CAA<1>	20 24 76
7	=MEM_A_A<6>		TRUE	MEM_A_CAA<2>	20 24 76
7	=MEM_A_A<8>		TRUE	MEM_A_CAA<3>	20 24 76
7	=MEM_A_A<7>		TRUE	MEM_A_CAA<4>	20 24 76
7	=MEM_A_BA<2>		TRUE	MEM_A_CAA<5>	20 24 76
7	=MEM_A_A<12>		TRUE	MEM_A_CAA<6>	20 24 76
7	=MEM_A_A<11>		TRUE	MEM_A_CAA<7>	20 24 76
7	=MEM_A_A<15>		TRUE	MEM_A_CAA<8>	20 24 76
7	=MEM_A_A<14>		TRUE	MEM_A_CAA<9>	20 24 76
7	=MEM_A_A<13>		TRUE	MEM_A_CAB<0>	21 24 76
7	=MEM_A_CAS_L		TRUE	MEM_A_CAB<1>	21 24 76
7	=MEM_A_WE_L		TRUE	MEM_A_CAB<2>	21 24 76
7	=MEM_A_RAS_L		TRUE	MEM_A_CAB<3>	21 24 76
7	=MEM_A_BA<0>		TRUE	MEM_A_CAB<4>	21 24 76
7	=MEM_A_A<2>		TRUE	MEM_A_CAB<5>	21 24 76
7	=MEM_A_BA<1>		TRUE	MEM_A_CAB<6>	21 24 76
7	=MEM_A_A<10>		TRUE	MEM_A_CAB<7>	21 24 76
7	=MEM_A_A<1>		TRUE	MEM_A_CAB<8>	21 24 76
7	=MEM_A_A<0>		TRUE	MEM_A_CAB<9>	21 24 76
7	=MEM_A_ODT<0>		TRUE	MEM_A_ODT<0>	20 21 24 76
7	=MEM_A_A<3>		TRUE	TP_LPDDR3_RSVD1	
7	=MEM_A_A<4>		TRUE	TP_LPDDR3_RSVD2	
7	=MEM_B_A<5>		TRUE	MEM_B_CAA<0>	22 24 76
7	=MEM_B_A<9>		TRUE	MEM_B_CAA<1>	22 24 76
7	=MEM_B_A<6>		TRUE	MEM_B_CAA<2>	22 24 76
7	=MEM_B_A<8>		TRUE	MEM_B_CAA<3>	22 24 76
7	=MEM_B_A<7>		TRUE	MEM_B_CAA<4>	22 24 76
7	=MEM_B_BA<2>		TRUE	MEM_B_CAA<5>	22 24 76
7	=MEM_B_A<12>		TRUE	MEM_B_CAA<6>	22 24 76
7	=MEM_B_A<11>		TRUE	MEM_B_CAA<7>	22 24 76
7	=MEM_B_A<15>		TRUE	MEM_B_CAA<8>	22 24 76
7	=MEM_B_A<14>		TRUE	MEM_B_CAA<9>	22 24 76
7	=MEM_B_A<13>		TRUE	MEM_B_CAB<0>	23 24 76
7	=MEM_B_CAS_L		TRUE	MEM_B_CAB<1>	23 24 76
7	=MEM_B_WE_L		TRUE	MEM_B_CAB<2>	23 24 76
7	=MEM_B_RAS_L		TRUE	MEM_B_CAB<3>	23 24 76
7	=MEM_B_BA<0>		TRUE	MEM_B_CAB<4>	23 24 76
7	=MEM_B_A<2>		TRUE	MEM_B_CAB<5>	23 24 76
7	=MEM_B_BA<1>		TRUE	MEM_B_CAB<6>	23 24 76
7	=MEM_B_A<10>		TRUE	MEM_B_CAB<7>	23 24 76
7	=MEM_B_A<1>		TRUE	MEM_B_CAB<8>	23 24 76
7	=MEM_B_A<0>		TRUE	MEM_B_CAB<9>	23 24 76
7	=MEM_B_ODT<0>		TRUE	MEM_B_ODT<0>	22 23 24 76
7	=MEM_B_A<3>		TRUE	TP_LPDDR3_RSVD3	
7	=MEM_B_A<4>		TRUE	TP_LPDDR3_RSVD4	

UNUSED MEMORY SIGNALS

		MAKE_BASE		
6	=MEM_RESET_L		TRUE	TP_CPU_MEM_RESET_L

Memory Bit/Byte Swizzle

		TRUE						TRUE			
76 71 7	MEM_A_DQ<0>		=MEM_A_DQ<7>	20	76 71 7	MEM_B_DQ<0>		=MEM_B_DQ<7>	22
76 71 7	MEM_A_DQ<1>		=MEM_A_DQ<6>	20	76 71 7	MEM_B_DQ<1>		=MEM_B_DQ<6>	22
76 71 7	MEM_A_DQ<2>		=MEM_A_DQ<5>	20	76 71 7	MEM_B_DQ<2>		=MEM_B_DQ<5>	22
76 71 7	MEM_A_DQ<3>		=MEM_A_DQ<1>	20	76 71 7	MEM_B_DQ<3>		=MEM_B_DQ<1>	22
76 71 7	MEM_A_DQ<4>		=MEM_A_DQ<3>	20	76 71 7	MEM_B_DQ<4>		=MEM_B_DQ<3>	22
76 71 7	MEM_A_DQ<5>		=MEM_A_DQ<2>	20	76 71 7	MEM_B_DQ<5>		=MEM_B_DQ<2>	22
76 71 7	MEM_A_DQ<6>		=MEM_A_DQ<0>	20	76 71 7	MEM_B_DQ<6>		=MEM_B_DQ<0>	22
76 71 7	MEM_A_DQ<7>		=MEM_A_DQ<4>	20	76 71 7	MEM_B_DQ<7>		=MEM_B_DQ<4>	22
76 71 7	MEM_A_DQ<8>		=MEM_A_DQ<10>	20	76 71 7	MEM_B_DQ<8>		=MEM_B_DQ<10>	22
76 71 7	MEM_A_DQ<9>		=MEM_A_DQ<14>	20	76 71 7	MEM_B_DQ<9>		=MEM_B_DQ<14>	22
76 71 7	MEM_A_DQ<10>		=MEM_A_DQ<8>	20	76 71 7	MEM_B_DQ<10>		=MEM_B_DQ<8>	22
76 71 7	MEM_A_DQ<11>		=MEM_A_DQ<9>	20	76 71 7	MEM_B_DQ<11>		=MEM_B_DQ<9>	22
76 71 7	MEM_A_DQ<12>		=MEM_A_DQ<15>	20	76 71 7	MEM_B_DQ<12>		=MEM_B_DQ<15>	22
76 71 7	MEM_A_DQ<13>		=MEM_A_DQ<11>	20	76 71 7	MEM_B_DQ<13>		=MEM_B_DQ<11>	22
76 71 7	MEM_A_DQ<14>		=MEM_A_DQ<12>	20	76 71 7	MEM_B_DQ<14>		=MEM_B_DQ<12>	22
76 71 7	MEM_A_DQ<15>		=MEM_A_DQ<13>	20	76 71 7	MEM_B_DQ<15>		=MEM_B_DQ<13>	22
76 71 7	MEM_A_DQ<16>		=MEM_A_DQ<21>	20	76 71 7	MEM_B_DQ<16>		=MEM_B_DQ<22>	22
76 71 7	MEM_A_DQ<17>		=MEM_A_DQ<16>	20	76 71 7	MEM_B_DQ<17>		=MEM_B_DQ<18>	22
76 71 7	MEM_A_DQ<18>		=MEM_A_DQ<23>	20	76 71 7	MEM_B_DQ<18>		=MEM_B_DQ<17>	22
76 71 7	MEM_A_DQ<19>		=MEM_A_DQ<18>	20	76 71 7	MEM_B_DQ<19>		=MEM_B_DQ<16>	22
76 71 7	MEM_A_DQ<20>		=MEM_A_DQ<19>	20	76 71 7	MEM_B_DQ<20>		=MEM_B_DQ<23>	22
76 71 7	MEM_A_DQ<21>		=MEM_A_DQ<22>	20	76 71 7	MEM_B_DQ<21>		=MEM_B_DQ<19>	22
76 71 7	MEM_A_DQ<22>		=MEM_A_DQ<17>	20	76 71 7	MEM_B_DQ<22>		=MEM_B_DQ<20>	22
76 71 7	MEM_A_DQ<23>		=MEM_A_DQ<20>	20	76 71 7	MEM_B_DQ<23>		=MEM_B_DQ<21>	22
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76 71 7	MEM_A_DQ<29>		=MEM_A_DQ<31>	20	76 71 7	MEM_B_DQ<29>		=MEM_B_DQ<30>	22
76 71 7	MEM_A_DQ<30>		=MEM_A_DQ<24>	20	76 71 7	MEM_B_DQ<30>		=MEM_B_DQ<29>	22
76 71 7	MEM_A_DQ<31>		=MEM_A_DQ<28>	20	76 71 7	MEM_B_DQ<31>		=MEM_B_DQ<25>	22
76 71 7	MEM_A_DQ<32>		=MEM_A_DQ<38>	21	76 71 7	MEM_B_DQ<32>		=MEM_B_DQ<39>	23
76 71 7	MEM_A_DQ<33>		=MEM_A_DQ<39>	21	76 71 7	MEM_B_DQ<33>		=MEM_B_DQ<38>	23
76 71 7	MEM_A_DQ<34>		=MEM_A_DQ<37>	21	76 71 7	MEM_B_DQ<34>		=MEM_B_DQ<37>	23
76 71 7	MEM_A_DQ<35>		=MEM_A_DQ<33>	21	76 71 7	MEM_B_DQ<35>		=MEM_B_DQ<33>	23
76 71 7	MEM_A_DQ<36>		=MEM_A_DQ<35>	21	76 71 7	MEM_B_DQ<36>		=MEM_B_DQ<35>	23
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76 71 7	MEM_A_DQ<46>		=MEM_A_DQ<44>	21	76 71 7	MEM_B_DQ<46>		=MEM_B_DQ<44>	23
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76 71 7	MEM_A_DQ<48>		=MEM_A_DQ<61>	21	76 71 7	MEM_B_DQ<48>		=MEM_B_DQ<53>	23
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76 71 7	MEM_A_DQ<50>		=MEM_A_DQ<58>	21	76 71 7	MEM_B_DQ<50>		=MEM_B_DQ<49>	23
76 71 7	MEM_A_DQ<51>		=MEM_A_DQ<62>	21	76 71 7	MEM_B_DQ<51>		=MEM_B_DQ<54>	23
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76 71 7	MEM_A_DQ<54>		=MEM_A_DQ<57>	21	76 71 7	MEM_B_DQ<54>		=MEM_B_DQ<48>	23
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76 71 7	MEM_A_DQ<63>		=MEM_A_DQ<50>	21	76 71 7	MEM_B_DQ<63>		=MEM_B_DQ<59>	23

20	=MEM_A_DQS_P<0>	TRUE	MEM_A_DQS_P<0>	7 76	22 =MEM_B_DQS_P<0> TRUE MEM_B_DQS_P<0> 7 76
20	=MEM_A_DQS_N<0>	TRUE	MEM_A_DQS_N<0>	7 76	22 =MEM_B_DQS_N<0> TRUE MEM_B_DQS_N<0> 7 76
20	=MEM_A_DQS_P<1>	TRUE	MEM_A_DQS_P<1>	7 76	22 =MEM_B_DQS_P<1> TRUE MEM_B_DQS_P<1> 7 76
20	=MEM_A_DQS_N<1>	TRUE	MEM_A_DQS_N<1>	7 76	22 =MEM_B_DQS_N<1> TRUE MEM_B_DQS_N<1> 7 76
20	=MEM_A_DQS_P<2>	TRUE	MEM_A_DQS_P<2>	7 76	22 =MEM_B_DQS_P<2> TRUE MEM_B_DQS_P<2> 7 76
20	=MEM_A_DQS_N<2>	TRUE	MEM_A_DQS_N<2>	7 76	22 =MEM_B_DQS_N<2> TRUE MEM_B_DQS_N<2> 7 76
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20	=MEM_A_DQS_N<3>	TRUE	MEM_A_DQS_N<3>	7 76	22 =MEM_B_DQS_N<3> TRUE MEM_B_DQS_N<3> 7 76
21	=MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<4>	7 76	23 =MEM_B_DQS_P<4> TRUE MEM_B_DQS_P<4> 7 76
21	=MEM_A_DQS_N<4>	TRUE	MEM_A_DQS_N<4>	7 76	23 =MEM_B_DQS_N<4> TRUE MEM_B_DQS_N<4> 7 76
21	=MEM_A_DQS_P<5>	TRUE	MEM_A_DQS_P<5>	7 76	23 =MEM_B_DQS_P<5> TRUE MEM_B_DQS_P<5> 7 76
21	=MEM_A_DQS_N<5>	TRUE	MEM_A_DQS_N<5>	7 76	23 =MEM_B_DQS_N<5> TRUE MEM_B_DQS_N<5> 7 76
21	=MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<7>	7 76	23 =MEM_B_DQS_P<6> TRUE MEM_B_DQS_P<6> 7 76
21	=MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<7>	7 76	23 =MEM_B_DQS_N<6> TRUE MEM_B_DQS_N<6> 7 76
21	=MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<6>	7 76	23 =MEM_B_DQS_P<7> TRUE MEM_B_DQS_P<7> 7 76
21	=MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<6>	7 76	23 =MEM_B_DQS_N<7> TRUE MEM_B_DQS_N<7> 7 76

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Functional Test Points

J6050 (LEFT FAN CONN)
FUNC_TEST
PP5V_S0 (3 TPs per Fan)
FAN_LT_PWM
FAN_LT_TACH

J4002 (ALS/CAMERA CONN)
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
PP5V_S3RS0_ALSCAM_F
MIPI_CLK_CONN_N
MIPI_CLK_CONN_P
CAM_SENSOR_WAKE_L_CONN
MIPI_DATA_CONN_N
MIPI_DATA_CONN_P
I2C_CAM_SCK
I2C_CAM_SDA

J9500 (RIO POWER PINS)
PP3V3_S4
PP5V_S3
PP1V5_S0
GND

SMBUS_PCH_CLK
SMBUS_PCH_DATA

J7715 (KBD BACKLIGHT CONN)
PPVOUT_S0_KBDBKLT
KBDLED_CATHODE1
KBDLED_CATHODE2

J7050 (MAIN BATT CONN)
PPVBAT_G3H_CONN
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA

SYS_DETECT_L

J6601 (2 MIC CONN)
CON_DMIC_PWR
CON_DMIC_SDA1
CON_DMIC_CLK

PCH_VSS_NCTF<19>
PCH_VSS_NCTF<19>

J4600 (LEFT USB CONN)
PP5V_S3_LTUSB_A_F
USB_LT1_N
USB_LT1_P

FUNC_TEST
GND
GND
GND
6 TPs

U0500 CHARZ TPS
PCIE_TBT_D2R_P<0> — PPA400
PCIE_TBT_D2R_N<0> — PPA401
PCIE_CLK100M_TBT_P — PPA423
PCIE_CLK100M_TBT_N — PPA424
PCIE_CAMERA_D2R_P — PPA402
PCIE_CAMERA_D2R_N — PPA403
PCIE_SSD_D2R_P<0> — PPA404
PCIE_SSD_D2R_N<0> — PPA405
PCIE_AP_D2R_P — PPA410
PCIE_AP_D2R_N — PPA411
USB3RPCIE_SD_D2R_P — PPA420
USB3RPCIE_SD_D2R_N — PPA421
HDA_SDIN0 — PPA408 (PLACE_NEAR=U0500.AY10:6MM)
MIPI_CLK_N — PPA441
MIPI_CLK_P — PPA442
MIPI_DATA_N — PPA443
MIPI_DATA_P — PPA444

U5000 CHARZ TPS
LPC_CLK24M_SMC — PPA419

J6601 (AUDIO 2-MIKE CONN)
DMIC_SDA3
DMIC_SDA2
DMIC_CLK3

J6602 (AUDIO LEFT SPEAKER CONN)
SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6603 (AUDIO RIGHT SPEAKER CONN)
SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N
GND

J8300 (EDP CONN)
PP5VR3V3_SW_LCD
PPVOUT_S0_LCDBKLT (2 TP needed)
I2C_BKLT_SCL
I2C_BKLT_SDA
LCD_HPD_CONN
LCD_IRQ_L
EDP_BKLT_PWM
=I2C_TCON_SCL
=I2C_TCON_SDA
EDP_PANEL_PWR_OR_PSR_EN
DP_INT_AUX_P
DP_INT_AUX_N
DP_INT_ML_P<0>
DP_INT_ML_N<0>
DP_INT_ML_P<1>
DP_INT_ML_N<1>
DP_INT_ML_P<2>
DP_INT_ML_N<2>
DP_INT_ML_P<3>
DP_INT_ML_N<3>

J4813 (KEY BOARD CONN)
PP3V3_S4
PP3V42_G3H
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6
WS_KBD7
WS_KBD8
WS_KBD9
WS_KBD10
WS_KBD11
WS_KBD12
WS_KBD13
WS_KBD14
WS_KBD15_CAP
WS_KBD16_NUM
WS_KBD17
WS_KBD18
WS_KBD19
WS_KBD20
WS_KBD21
WS_KBD22
WS_KBD23
WS_KBD_ONOFF_L
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD

J4802 (TPAD CONN)
SMBUS_SMC_2_S3_SDA
SMBUS_SMC_2_S3_SCL
=PPVIN_S4_TPAD
TPAD_ACTUATOR_EN_L
TPAD_ACTUATOR_THRMTRIP_L
=TPAD_WAKE_L
SMC_LID
=PP3V3_S4_TPAD
I2C_IOXP_SDA
I2C_IOXP_SCL
TPAD_SPI_INT_L
=TPAD_SPI_SCLK
=TPAD_SPI_MISO
=TPAD_SPI_MOSI
TPAD_VBUS_EN
PP5V_S4_TPAD_F
IOXP2_INT_L
=TPAD_SPI_BUS_EN
=TPAD_SPI_CS_L
GND_ACTUATOR
USB_TPAD_P
USB_TPAD_N
=I2C_TPAD_SCL
=I2C_TPAD_SDA

J7000 (DC POWER CONN)
TDM_ONEWIRE_MPM
ADAPTER_SENSE
PP18V5_DCIN_FUSE
GND
PM_CLKRUN_L
PM_SYSRST_L
SMC_ONOFF_L

J6100 (LPC + SPI CONN)
PP3V42_G3H
PP5V_S0
LPC_AD<0>
LPC_AD<2>
LPC_AD<1>
LPC_AD<3>
LPCPLUS_GPIO
LPCPLUS_RESET_L
SMC_TDO
SMC_TX_L
LPC_FRAME_L
SPIROM_USE_MLB
PM_CLKRUN_L
LPC_SERIRQ
LPC_PWRDWN_L
SMC_TDI
SMC_TCK
SMC_RESET_L
SMC_ROMBOOT
SMC_RX_L
SMC_TMS

ICT Test Points

POWER RAILS
FUNC_TEST
PM_SLP_S3_L
PP0V6_S0_DDRVTT
PP1V05_S0
GND (4 TPS)
PP3V3_S0
PP3V3_S3
PP3V3_S5
PP3V3_S5_AVREF_SMC
PP3V42_G3H
PP5V_S0
PP5V_S3
PP5V_S5
PPBUS_G3H
PPDCIN_G3H
PPVCC_S0_CPU
PPVTTDDR_S3 — TP_PM_SLP_A_L (MAKE_BASE=TRUE) — NC_PM_SLP_A_L

NO_TESTS
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0_R
TBTBPWRSW_ISET_S3
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTAPWRSW_ISET_S3_R
TBT_A_R2D_C_P<1..0>
TBT_A_R2D_C_N<1..0>
TBT_A_R2D_P<1..0>
TBT_A_R2D_N<1..0>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_B_R2D_C_P<1..0>
TBT_B_R2D_C_N<1..0>
TBT_B_R2D_P<1..0>
TBT_B_R2D_N<1..0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
TBT_B_D2R_C_P<1>
TBT_B_D2R_C_N<1>
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_AP_R2D_P
PCIE_AP_R2D_N

MEM_A_DQ<63..0>
PPVTTDDR_S3
MEM_B_DQ<63..0>

HDMI_IG_CLK_C_P
HDMI_IG_CLK_C_N
HDMI_IG_DATA_C_P<2..0>
HDMI_IG_DATA_C_N<2..0>

TP_XDP_PCH_HOOK4 — NC_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5 — NC_XDP_PCH_HOOK5
TP_XDP_PCH_OBSFN_B<0> — NC_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1> — NC_XDP_PCH_OBSFN_B<1>
TP_XDP_PCH_OBSFN_A<0> — NC_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1> — NC_XDP_PCH_OBSFN_A<1>
TP_XDP_PCH_OBSFN_D<0> — NC_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_D<1> — NC_XDP_PCH_OBSFN_D<1>
TP_XDP_PCH_TRST_L — NC_XDP_PCH_TRST_L
TP_1V05_S0_PCH_VCCAPLLEXP — NC_1V05_S0_PCH_VCCAPLLEXP
TP_AUD_CODEC_MICBIAS — NC_AUD_CODEC_MICBIAS
TP_AUD_MIC_INRP — NC_AUD_MIC_INRP
TP_AUD_MIC_INRN — NC_AUD_MIC_INRN

NC_AUD_LO1_LN
NC_AUD_LO1_LP
NC_AUD_LO1_RN
NC_AUD_LO1_RP
NC_AUD_LO4_LN
NC_AUD_LO4_LP
NC_AUD_LO4_RN
NC_AUD_LO4_RP
NC_CS4208_GPO0
NC_CS4208_GPO1
NC_CS4208_LRCLKA
NC_CS4208_LRCLKB
NC_CS4208_MCLKA
NC_CS4208_MCLKB
NC_CS4208_SCLKA
NC_CS4208_SCLKB
NC_CS4208_SDOUTA
NC_CS4208_SDOUTB
NC_DMIC_CLK0
NC_DMIC_CLK1
NC_DMIC_CLK2

NC_SMC_HIB_L
NC_SMC_XOSC1

NC NO_TEST

High Speed NO_TEST
PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_SSD_R2D_C_P<3..0>
PCIE_SSD_R2D_C_N<3..0>
PCIE_SSD_R2D_P<3..0>
PCIE_SSD_R2D_N<3..0>
PCIE_SSD_D2R_P<3..0>
PCIE_SSD_D2R_N<3..0>
PCIE_TBT_R2D_C_P<3..0>
PCIE_TBT_R2D_C_N<3..0>
PCIE_TBT_R2D_P<3..0>
PCIE_TBT_R2D_N<3..0>
PCIE_TBT_D2R_P<3..1>
PCIE_TBT_D2R_N<3..1>
PCIE_TBT_D2R_C_P<3..1>
PCIE_TBT_D2R_C_N<3..1>
USB3_EXTA_D2R_P
USB3_EXTA_D2R_N
USB3_EXTA_R2D_C_P
USB3_EXTA_R2D_C_N
USB3_EXTA_R2D_N
USB3_EXTA_R2D_N
USB3_EXTB_D2R_P
USB3_EXTB_D2R_N
USB3_EXTB_R2D_C_P
USB3_EXTB_R2D_C_N
PCIE_CLK100M_SSD_P
PCIE_CLK100M_SSD_N
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_CAMERA_P
PCIE_CLK100M_CAMERA_N

Unused nets with offpage
(Nets with offpages not used on this project)
HDD_PWR_EN
WOL_EN
BT_PWRRST_L
ENET_MEDIA_SENSE
ODD_PWR_EN_L
ENET_LOW_PWR
AUD_IP_PERIPHERAL_DET
AUD_IPHS_SWITCH_EN
ENETSD_CLKREQ_L

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X304 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA,BGA_MEM	MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.120 MM	0.120 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.120 MM	0.120 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.155 MM	0.155 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
73_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.110 MM	0.110 MM		0.120 MM	0.120 MM
73_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.110 MM		0.120 MM	0.120 MM
73_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.141 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal
Inner dielectric is 0.053 mm nominal

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	-	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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PCB Rule Definitions

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
XDP_TCK0	CPU_45S	CPU_18MIL	XDP_CPU_TCK	6 16
XDP_TCK0	CPU_45S	CPU_18MIL	PCH_JTAGX	12 16
XDP_TCK1	CPU_45S	CPU_18MIL	XDP_PCH_TCK	12 16
XDP_TDO	CPU_45S		XDP_CPU_TDO	6 16
XDP_TDO	CPU_45S		XDP_PCH_TDO	12 16
XDP_TDI	CPU_45S		XDP_CPU_TDI	6 16
XDP_TDI	CPU_45S		XDP_PCH_TDI	12 16
XDP_TMS	CPU_45S		XDP_CPU_TMS	6 16
XDP_TMS	CPU_45S		XDP_PCH_TMS	12 16
XDP_TRST_L	CPU_45S		XDP_TRST_L	16
XDP_TRST_L	CPU_45S		XDP_CPUPCH_TRST_L	16
XDP_PRDY_L	CPU_45S		XDP_CPU_PRDY_L	6 16
XDP_PREQ_L	CPU_45S		XDP_CPU_PREQ_L	6 16
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	CPU_VCCST_PWRGD	8 16 17
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	XDP_CPU_VCCST_PWRGD	16
CPU_BPM	CPU_45S	CPU_08MIL	XDP_BPM_L<1..0>	6 16
CPU_BPM_TP	CPU_45S		XDP_BPM_L<7..2>	6 16
CPU_RCOMP_SM	CPU_27P4S	CPU_25MIL	CPU_SM_RCOMP<2..0>	6
CPU_RCOMP_EDP	CPU_27P4S	CPU_25MIL	MCP_EDP_RCOMP	5
CPU_RCOMP_OPI	CPU_27P4S	CPU_12MIL	CPU_OPI_RCOMP	6
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU_PROCHOT_L	6 38 39 55
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU_PROCHOT_R_L	6
CPU_CATERR	CPU_45S	CPU_08MIL	CPU_CATERR_L	6 38
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU_VIDALERT_L	8 55
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU_VIDALERT_R_L	8
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU_VIDSCLK	8 55
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU_VIDSCLK_R	8
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU_VIDSOUT	8 55
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU_VIDSOUT_R	8
CPU_PECI	CPU_45S	CPU_18MIL	CPU_PECI	6 39
CPU_PECI	CPU_45S	CPU_18MIL	CPU_PECI_R	38 39
CPU_PECI	CPU_45S	CPU_18MIL	SMC_PECI_L	38 39
CPU_PECI	CPU_45S	CPU_18MIL	SMC_PECI_L_R	39
CPU_CFG	CPU_45S		CPU_CFG<19..11>	6 16
CPU_CFG_PD	CPU_45S		CPU_CFG<10..8>	6 16
CPU_CFG	CPU_45S		CPU_CFG<7..5>	6 16
CPU_CFG_PD	CPU_45S		CPU_CFG<4>	6 16
CPU_CFG_3	CPU_45S		CPU_CFG<3>	6 16
CPU_CFG	CPU_45S		CPU_CFG<2>	6 16
CPU_CFG_PD	CPU_45S		CPU_CFG<1..0>	6 16
CPU_MEM_RESET	CPU_45S	CPU_08MIL	MEM_RESET_L	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 55
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 55

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USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5x_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
USB_BT	USB_85D	USB	USB_BT_P	14 31
USB_BT	USB_85D	USB	USB_BT_N	14 31
USB_BT	USB_85D	USB	USB_BT_CONN_P	31 66
USB_BT	USB_85D	USB	USB_BT_CONN_N	31 66
USB_EXTA	USB_85D	USB	USB_EXTA_P	14 35
USB_EXTA	USB_85D	USB	USB_EXTA_N	14 35
	DEFAULT	DEFAULT	SMC_DEBUGPRT_RX_L	35 38 39
	DEFAULT	DEFAULT	SMC_DEBUGPRT_TX_L	35 38 39
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_P	35
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_N	35
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_F_P	35
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_F_N	35
USB_EXTA	USB_85D	USB	USB_LT1_P	71
USB_EXTA	USB_85D	USB	USB_LT1_N	71
USB_EXTB	USB_85D	USB	USB_EXTB_P	14 66
USB_EXTB	USB_85D	USB	USB_EXTB_N	14 66
USB_TPAD (TS31)	USB_85D	USB	USB_TPAD_P	14 36 71
USB_TPAD (TS30)	USB_85D	USB	USB_TPAD_N	14 36 71
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3_EXTA_D2R_P	14 35 71
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3_EXTA_D2R_N	14 35 71
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_P	35
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_N	35 71
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_C_P	14 35 71
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_C_N	14 35 71
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_P	14 66 71
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_N	14 66 71
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_P	14 66 71
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_N	14 66 71
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_P	14 66 71
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_N	14 66 71
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_P	14 66
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_N	14 66
USB_NC	USB_85D	USB	NC_USB_IRP	69
USB_NC	USB_85D	USB	NC_USB_IRN	69
USB_NC	USB_85D	USB	NC_USB_5P	69
USB_NC	USB_85D	USB	NC_USB_5N	69
USB_NC	USB_85D	USB	NC_USB_SDP	69
USB_NC	USB_85D	USB	NC_USB_SDN	69
USB_NC	USB_85D	USB	NC_USB_CAMERAP	69
USB_NC	USB_85D	USB	NC_USB_CAMERAN	69
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	14
	SATA_85D	SATA_RX	DUMMY_SATA_D2R_P	
	SATA_85D	SATA_RX	DUMMY_SATA_D2R_N	
	SATA_85D	SATA_TX	DUMMY_SATA_R2D_P	
	SATA_85D	SATA_TX	DUMMY_SATA_R2D_N	
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	33 34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	33 34
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 25
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	25

Notes:
This is here to keep the SATA rules.

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 38 71
LPC_AD	LPC_45S	LPC	LPC_FRAME_L	14 38 71
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 71
SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_CLK	14 41 71
SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_DATA	14 41 71
SMI_PCH_0	SMB_45S	SMB	SML_PCH_0_CLK	14 41
SMI_PCH_0	SMB_45S	SMB	SML_PCH_0_DATA	14 41
	SMB_45S	SMB	SML_PCH_1_CLK	14 41
	SMB_45S	SMB	SML_PCH_1_DATA	14 41
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 49
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 49
HDA_SYNC	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST	HDA_45S	HDA	HDA_RST_R_L	12
HDA_RST	HDA_45S	HDA	HDA_RST_L	12 49
HDA_SDIN	HDA_45S	HDA	HDA_SDIN0	12 49 71
HDA_SDIN	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	49
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 49
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT_R	12 17
SPI_MLB	SPI_45S	SPI	SPI_ALT_CLK	47
SPI_MLB	SPI_45S	SPI	SPI_CLK	47
SPI_MLB	SPI_45S	SPI	SPI_CLK_R	14 47
SPI_MLB	SPI_45S	SPI	SPI_MLB_CLK	47
SPI_MLB	SPI_45S	SPI	SPI_SMC_CLK	38 47
SPI_MLB	SPI_45S	SPI	SPI_ALT_CS_L	47
SPI_MLB	SPI_45S	SPI	SPI_CS0_L	47
SPI_MLB	SPI_45S	SPI	SPI_CS0_R_L	14 47
SPI_MLB	SPI_45S	SPI	SPI_MLB_CS_L	47
SPI_MLB	SPI_45S	SPI	SPI_SMC_CS_L	38 47
SPI_MLB	SPI_45S	SPI	SPI_ALT_IO1_MISO	47
SPI_MLB	SPI_45S	SPI	SPI_MISO	14 47
SPI_MLB	SPI_45S	SPI	SPI_MISO_R	47
SPI_MLB	SPI_45S	SPI	SPI_MLB_IO1_MISO	47
SPI_MLB	SPI_45S	SPI	SPI_SMC_MISO	38 47
SPI_MLB	SPI_45S	SPI	SPI_ALT_IO0_MOSI	47
SPI_MLB	SPI_45S	SPI	SPI_MOSI	47
SPI_MLB	SPI_45S	SPI	SPI_MOSI_R	14 47
SPI_MLB	SPI_45S	SPI	SPI_MLB_IO0_MOSI	47
SPI_MLB	SPI_45S	SPI	SPI_SMC_MOSI	38 47
SPI_MLB_IO2	SPI_45S	SPI	SPI_IO<2>	14 47
1.8V SPI_MLB_IO2	SPI_45S	SPI	SPI_IO2_R	47
SPI_MLB_IO2	SPI_45S	SPI	SPI_MLB_IO2_WP_L	47
1.8V SPI_MLB_IO2	SPI_45S	SPI	SPI_ALT_IO2_WP_L	47
SPI_MLB_IO3	SPI_45S	SPI	SPI_IO<3>	14 47
1.8V SPI_MLB_IO3	SPI_45S	SPI	SPI_IO3_R	47
SPI_MLB_IO3	SPI_45S	SPI	SPI_MLB_IO3_HOLD_L	47
1.8V SPI_MLB_IO3	SPI_45S	SPI	SPI_ALT_IO3_HOLD_L	47
1.8V SPI_TPAD	SPI_45S	SPI	TPAD_SPI_CLK	15 37
1.8V SPI_TPAD_CS	SPI_45S	SPI	TPAD_SPI_CS_L	15 37
1.8V SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MISO	15 37
1.8V SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MOSI	15 37
PCH_RTCX	PCH_45S	PCH_15MIL	PCH_CLK32K_RTCX1	12 17
PCH_SRTCRST	PCH_45S	PCH_15MIL	PCH_SRTCRST_L	12
PCH_RTCRST	PCH_45S	PCH_15MIL	RTC_RESET_L	12
PCH_THRMTRIP	PCH_45S	PCH_18MIL	PM_THRMTRIP_L	15 39
PCH_THRMTRIP	PCH_45S	PCH_18MIL	PM_THRMTRIP_R_L	39
	PCH_45S	PCH_15MIL	PCH_INTRUDER_L	12
	PCH_45S	PCH_15MIL	PCH_INTVRMEN	12
	PCH_45S	PCH_15MIL	PCH_DSWVRMEN	13
	PCH_45S	PCH_15MIL	PM_RSMRST_L	13 64
	PCH_45S	PCH_15MIL	PM_SYSRST_L	13 17 38 71
	PCH_45S	PCH_15MIL	XDP_DBRESET_L	16 17
	PCH_45S	PCH_15MIL	PM_PCH_SYS_PWROK	13 16 17 38
	PCH_45S	PCH_15MIL	XDP_SYS_PWROK	16
	PCH_45S	PCH_15MIL	SYS_PWROK_R	17
	PCH_45S	PCH_15MIL	PM_PCH_PWROK	13 17
	PCH_45S	PCH_15MIL	PM_S0_PGOOD	17
	PCH_45S	PCH_15MIL	SMC_DELAYED_PWRGD	17 26 27 38 39
	PCH_45S	PCH_15MIL	PM_DSW_PWRGD	13 38
	PCH_45S	PCH_15MIL	PM_PWRBTN_L	13 16 38
	PCH_45S	PCH_15MIL	XDP_CPU_PWRBTN_L	16
	PCH_45S	PCH_15MIL	PCIE_WAKE_L	13 31 33
	PCH_45S	PCH_15MIL	AP_PCIE_WAKE_L	31 66
	PCH_45S	PCH_15MIL	CAM_PCIE_WAKE_L	33
	PCH_45S	PCH_15MIL	TBT_CIO_PLUG_EVENT_L	18 25
PCH_CLK24M_XTAL	PCH_45S	PCH_20MIL	PCH_CLK24M_XTALIN	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MIL	PCH_CLK24M_XTALOUT	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MIL	PCH_CLK24M_XTALOUT_R	17
PCH_RCOMP_PCIE	PCH_27P4S	PCH_12MIL	PCH_PCIE_RCOMP	14
PCH_RCOMP_OPI	PCH_27P4S	PCH_12MIL	PCH_OPI_COMP	15
PCH_RCOMP_SATA	PCH_27P4S	PCH_12MIL	PCH_SATA_RCOMP	12

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PCH Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	0.066 MM	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTL	*	=3x_DIELECTRIC	?
MEM_CTL2CTL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?
MEM_CMD2CMD_BM	*	=3x_DIELECTRIC	?
MEM_CMD2CTL_BM	*	=3x_DIELECTRIC	?
MEM_CTL2CTL_BM	*	=3x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTL2CTL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CMD2CMD_BM	TOP,BOTTOM	=3x_DIELECTRIC	?
MEM_CMD2CTL_BM	TOP,BOTTOM	=3x_DIELECTRIC	?
MEM_CTL2CTL_BM	TOP,BOTTOM	=3x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_BM
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_BM
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_BM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DQBYTE_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DQBYTE_7	*	MEM_DQS2OWNDATA

Broadwell ULT Memory Down LPDDR3 1x4 Length Matching

LPDDR3 Signal Group	Unit	Min Length	Max Length
CTL/CKEmax - CTL/CKEmin	mils	0	50
CTL/CKE to CLK	mils	CLK - 100	0
(CMDmax - CMDmin)	mils	0	50
CMD to CLK	mils	CLK - 250	CLK + 250
DQmax - DQmin per byte	mils	0	125
DQmax to DQs per byte	mils	DQS - 200	DQS + 50
DQS to DQS#	mils	-2.5	2.5
DQS to CLK (Rule 1)	mils	CLK - 750	CLK + 1250
CLK to CLK#	mils	-2.5	2.5

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	BGA_MEM	MEM_73D
MEM_40S	BGA_MEM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>	7 21 24
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_CS_L<1..0>	7 20 21 24
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_ODT<0>	20 21 24 70
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>	20 24 70
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>	21 24 70
MEM_A_DQBYTE0	MEM_40S	MEM_A_DQBYTE_0	MEM_A_DQ<7..0>	7 70 71
MEM_A_DQBYTE1	MEM_40S	MEM_A_DQBYTE_1	MEM_A_DQ<15..8>	7 70 71
MEM_A_DQBYTE2	MEM_40S	MEM_A_DQBYTE_2	MEM_A_DQ<23..16>	7 70 71
MEM_A_DQBYTE3	MEM_40S	MEM_A_DQBYTE_3	MEM_A_DQ<31..24>	7 70 71
MEM_A_DQBYTE4	MEM_40S	MEM_A_DQBYTE_4	MEM_A_DQ<39..32>	7 70 71
MEM_A_DQBYTE5	MEM_40S	MEM_A_DQBYTE_5	MEM_A_DQ<47..40>	7 70 71
MEM_A_DQBYTE6	MEM_40S	MEM_A_DQBYTE_6	MEM_A_DQ<55..48>	7 70 71
MEM_A_DQBYTE7	MEM_40S	MEM_A_DQBYTE_7	MEM_A_DQ<63..56>	7 70 71
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 70
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 70
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 70
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 70
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 70
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 70
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 70
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 70
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 70
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 70
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 70
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 70
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 70
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 70
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 70
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 70
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>	7 23 24
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_CS_L<1..0>	7 22 23 24
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_ODT<0>	22 23 24 70
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>	22 24 70
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>	23 24 70
MEM_B_DQBYTE0	MEM_40S	MEM_B_DQBYTE_0	MEM_B_DQ<7..0>	7 70 71
MEM_B_DQBYTE1	MEM_40S	MEM_B_DQBYTE_1	MEM_B_DQ<15..8>	7 70 71
MEM_B_DQBYTE2	MEM_40S	MEM_B_DQBYTE_2	MEM_B_DQ<23..16>	7 70 71
MEM_B_DQBYTE3	MEM_40S	MEM_B_DQBYTE_3	MEM_B_DQ<31..24>	7 70 71
MEM_B_DQBYTE4	MEM_40S	MEM_B_DQBYTE_4	MEM_B_DQ<39..32>	7 70 71
MEM_B_DQBYTE5	MEM_40S	MEM_B_DQBYTE_5	MEM_B_DQ<47..40>	7 70 71
MEM_B_DQBYTE6	MEM_40S	MEM_B_DQBYTE_6	MEM_B_DQ<55..48>	7 70 71
MEM_B_DQBYTE7	MEM_40S	MEM_B_DQBYTE_7	MEM_B_DQ<63..56>	7 70 71
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 70
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 70
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 70
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 70
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 70
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 70
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 70
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 70
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 70
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 70
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 70
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 70
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 70
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 70
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 70
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 70
		MEM_PWR	PP1V2_S3	68
		MEM_PWR	PP1V2_S3_CPUDDR	68
		MEM_PWR	PP0V6_S0_DDRVTT	68 71
		MEM_PWR	PPVTTDDR_S3	68 71
		MEM_12MIL	CPU_DIMMA_VREFDQ	7 19
		MEM_12MIL	CPU_DIMMB_VREFDQ	7 19
		MEM_12MIL	CPU_DIMM_VREFCA	7 19
		MEM_12MIL	PP0V6_S3_MEM_VREFDQ_A	20 21 68
		MEM_12MIL	PP0V6_S3_MEM_VREFDQ_B	22 23 68
		MEM_12MIL	PP0V6_S3_MEM_VREFCA_A	20 21 68
		MEM_12MIL	PP0V6_S3_MEM_VREFCA_B	22 23 68

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PAGE TITLE: Memory Constraints

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Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4x_DIELECTRIC	?
HDMIDATA_2SAME	*	=3x_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DPHDMI	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMIDATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMIDATA_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_2OTHER
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	HDMI_DATA	*	DP_2SAME
DISPLAYPORT	TBTDP_TX	*	DP_2SAME
DISPLAYPORT	TBTDP_RX	*	TBTDP_TXRX

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

Thunderbolt, DP, HDMI Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_C_P<1..0> 25 28 71
	TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_C_N<1..0> 25 28 71
	TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_P<1..0> 28 71
	TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_N<1..0> 28 71
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1> 25 28
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1> 25 28
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1> 28
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1> 28
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 28
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 28
1355	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3> 25 28
1354	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3> 25 28
1353	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3> 28
1352	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3> 28
	TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_P<0> 28 71
	TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_N<0> 28 71
	TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_P<0> 25 28 71
	TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_N<0> 25 28 71
1343	TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_P<1> 28 71
1342	TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_N<1> 28 71
1341	TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_P<1> 25 28 71
1340	TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_N<1> 25 28 71
	TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P 28
	TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N 28
	DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P 25 28
	DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N 25 28
	DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_P 28
	DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_N 28
	TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_C_P<1..0> 25 29 71
	TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_C_N<1..0> 25 29 71
	TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_P<1..0> 29 71
	TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_N<1..0> 29 71
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1> 25 29
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1> 25 29
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1> 29
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1> 29
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 29
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 29
1351	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3> 25 29
1350	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3> 25 29
1348	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3> 29
1349	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3> 29
	TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_P<0> 29 71
	TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_N<0> 29 71
	TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_P<0> 25 29 71
	TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_N<0> 25 29 71
1347	TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_P<1> 29 71
1346	TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_N<1> 29 71
1344	TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_P<1> 25 29 71
1345	TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_N<1> 25 29 71
	TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P 29
	TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N 29
	DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P 25 29
	DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N 25 29
	DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_P 29
	DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_N 29
1338	DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0> 5 25
1339	DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0> 5 25
1336	DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0> 25
1337	DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0> 25
1335	DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_C_P 13 25
1334	DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_C_N 13 25
1324	DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P 25
1333	DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N 25
1332	DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0> 25 67
1330	DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0> 25 67
1331	DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0> 25
1328	DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0> 25
1329	DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_C_P 25 67
1327	DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_C_N 25 67
1325	DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P 25
1326	DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N 25
1356	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0> 65
1360	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0> 65
1316	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0> 5 65
1358	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0> 5 65
1357	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0> 65 71
1359	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0> 65 71
1320	DP_INT_AUXCH	DP_85D		DP_INT_AUXCH_C_P 5 65
1321	DP_INT_AUXCH	DP_85D		DP_INT_AUXCH_C_N 5 65
1322	DP_INT_AUXCH	DP_85D		DP_INT_AUXCH_P 65 71
1323	DP_INT_AUXCH	DP_85D		DP_INT_AUXCH_N 65 71

Notes:
AUX and DDC was removed from DISPLAYPORT or TBTDP_RX/TX because it's not high speed, and to save routing space.

Only used on dual-port hosts.

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
SPI_TBT_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	25
SPI_TBT_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	25
SPI_TBT_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	25
SPI_TBT_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	25
1815 DP_HDMI_TBT_ML	DP_85D	DISPLAYPORT	DP_HDMI_TBT_ML_P<3..0>	67 69
1816 DP_HDMI_TBT_ML	DP_85D	DISPLAYPORT	DP_HDMI_TBT_ML_N<3..0>	67 69
1818 DP_HDMI_TBT_AUX	DP_85D		DP_HDMI_TBT_AUX_P	67 69
1817 DP_HDMI_TBT_AUX	DP_85D		DP_HDMI_TBT_AUX_N	67 69
1809 HDMI_CLOCK	HDMI_85D	HDMI_CLK	HDMI_IG_CLK_C_P	66 67 71
1808 HDMI_CLOCK	HDMI_85D	HDMI_CLK	HDMI_IG_CLK_C_N	66 67 71
1811 HDMI_DATA	HDMI_85D	HDMI_DATA	HDMI_IG_DATA_C_P<2..0>	66 67 71
1810 HDMI_DATA	HDMI_85D	HDMI_DATA	HDMI_IG_DATA_C_N<2..0>	66 67 71

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	33 34
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	33 34
S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	33 34
S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	33 34
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	33 34
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	33 34
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	33 34
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	33 34
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	33 34
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	33 34
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	33 34
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	33 34
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	33 34
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	33 34
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	33 34 71
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	33 34 71
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	34 71
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	34 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	33 34 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	33 34 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	34 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	34 71
		S2_MEM_PWR	PP1V35_CAM	33 34
		S2_MEM_PWR	PP0V675_CAM_VREF	33 34
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	34
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	34

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SMC SMBus & Charger Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	38 41 71
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	38 41 71
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	38 41 71
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	38 41 71
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	38 41
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	38 41
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	38 41 71
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	38 41 71
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SCL	38 41
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SDA	38 41

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO

X304 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
THERM_DP_TBT_D1	THERM_45S	THERM	TBTTHMSNS_D1_P	45
THERM_DP_TBT_D1	THERM_45S	THERM	TBTTHMSNS_D1_N	45
THERM_DP_CPU_D1	THERM_45S	THERM	CPUTHMSNS_D1_P	45
THERM_DP_CPU_D1	THERM_45S	THERM	CPUTHMSNS_D1_N	45
THERM_DP_CPU_D2	THERM_45S	THERM	CPUTHMSNS_D2_P	45
THERM_DP_CPU_D2	THERM_45S	THERM	CPUTHMSNS_D2_N	45
SENSE_DP	SENSE_45S	SENSE	ISNS_CPUDDR_P	43
SENSE_DP	SENSE_45S	SENSE	ISNS_CPUDDR_N	43
SENSE_DP_LCDBKLT	SENSE_45S	SENSE	ISNS_LCDBKLT_P	42 60
SENSE_DP_LCDBKLT	SENSE_45S	SENSE	ISNS_LCDBKLT_N	42 60
SENSE_DP_TBT	SENSE_45S	SENSE	ISNS_TBT_P	44
SENSE_DP_TBT	SENSE_45S	SENSE	ISNS_TBT_N	44
SENSE_DP	SENSE_45S	SENSE	ISNS_LCDPANEL_P	44 65
SENSE_DP	SENSE_45S	SENSE	ISNS_LCDPANEL_N	44 65
	SENSE_45S	SENSE	ISNS_HS_COMPUTING_P	42 44
	SENSE_45S	SENSE	ISNS_HS_COMPUTING_N	42 44
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER5V_P	42
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER5V_N	42
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER3V3_P	42
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER3V3_N	42
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_P	43
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_N	43
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_R_P	43
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_R_N	43
SENSE_DP	SENSE_45S	SENSE	ISNS_1V05_S0_P	43 59
SENSE_DP	SENSE_45S	SENSE	ISNS_1V05_S0_N	43 59
SENSE_DP	SENSE_45S	SENSE	ISNS_SSD_P	43
SENSE_DP	SENSE_45S	SENSE	ISNS_SSD_N	43
SENSE_DP	SENSE_45S	SENSE	ISNS_TPAD_P	42
SENSE_DP	SENSE_45S	SENSE	ISNS_TPAD_N	42
SENSE_DP	SENSE_45S	SENSE	ISNS_1V8_S3_P	43 61
SENSE_DP	SENSE_45S	SENSE	ISNS_1V8_S3_N	43 61
SENSE_DP	SENSE_45S	SENSE	ISNS_PP3V3S0_P	43
SENSE_DP	SENSE_45S	SENSE	ISNS_PP3V3S0_N	43
SENSE_DP	SENSE_45S	SENSE	ISNS_PP5VS0_P	43
SENSE_DP	SENSE_45S	SENSE	ISNS_PP5VS0_N	43
SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_P	44 45
SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_N	44 45
SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_R_P	44
SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_R_N	44
SENSE_DP_CHGR_CST	SENSE_45S	SENSE	CHGR_CSI_P	54
SENSE_DP_CHGR_CST	SENSE_45S	SENSE	CHGR_CSI_N	54
SENSE_DP_CHGR_CST	SENSE_45S	SENSE	CHGR_CSI_R_P	54
SENSE_DP_CHGR_CST	SENSE_45S	SENSE	CHGR_CSI_R_N	54
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_P	54
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_N	54
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_R_P	44 54
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_R_N	44 54

The signals below have no topologies assigned.

DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR_ISNS1_P	43 56
DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR_ISNS1_N	43 56
DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR_ISNS2_P	43 56
DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR_ISNS2_N	43 56

X304 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_L_P	48 50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_L_N	48 50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LIN_P	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LIN_N	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_LIN_P	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_LIN_N	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_R_P	48 50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_R_N	48 50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RIN_P	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RIN_N	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_RIN_P	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_RIN_N	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_L_P	48 50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_L_N	48 50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LSUBIN_P	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LSUBIN_N	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	LSUBIN_P	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	LSUBIN_N	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_R_P	48 50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_R_N	48 50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RSUBIN_P	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RSUBIN_N	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	RSUBIN_P	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	RSUBIN_N	50
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SL_OUT_P	50 52 71
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SL_OUT_N	50 52 71
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SR_OUT_P	50 52 71
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SR_OUT_N	50 52 71
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_L_OUT_P	50 52 71
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_L_OUT_N	50 52 71
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_R_OUT_P	50 52 71
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_R_OUT_N	50 52 71
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CH_HS_GND	48 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_HS_MIC_P	
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_SLEEVE	52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_SLEEVE_XW	51 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HP_PORT_REFCH	48 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HS_MIC_P	51 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	CODEC_HS_MIC_P	48
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	HS_MIC_P	48 51
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_HS_MIC_N	
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_RING2	52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_RING2_XW	51 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HP_PORT_REFUS	48 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HS_MIC_N	51 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_US_HS_GND	48 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	HS_MIC_N	48 51
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	CODEC_HS_MIC_N	48
		SB_POWER	PP3V3_S5	68 71
		SB_POWER	PP3V3_S0	68 71
		GND	GND	

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PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

PCI Express Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING	
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_P<3..1> 12 32 71
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_N<3..1> 12 32 71
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_P<0> 12 32 71
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_N<0> 12 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_C_P<3..0> 12 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_C_N<3..0> 12 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_P<3..0> 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_N<3..0> 32 71
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_P<0> 14 25 71
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_N<0> 14 25 71
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_P<0> 25
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_N<0> 25
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_P<3..1> 14 25 71
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_N<3..1> 14 25 71
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_P<3..1> 25 71
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_N<3..1> 25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_P<3..0> 25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_N<3..0> 25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_P<3..0> 14 25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_N<3..0> 14 25 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_P 66 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_N 66 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_C_P 14 66 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_C_N 14 66 71
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE_AP_D2R_P 14 66 71
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE_AP_D2R_N 14 66 71
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P 66
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N 66
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P 12 66 71
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N 12 66 71
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P 12 34 71
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N 12 34 71
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P 33 34
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N 33 34
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P 12 32 71
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N 12 32 71
180 PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_RC1_P 32
180 PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_RC1_N 32
180 PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_RC2_P 32
180 PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_RC2_N 32
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P 12 25 71
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N 12 25 71
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_P 14 34 71
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